

Sciclient Documentation

Release VERSION

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INTRODUCTION

1.1 Overview

Traditional Texas Instruments SoCs implement system control functions such as power management within operating systems on each of the processing units (ARM/DSP etc). However the traditional approach has had tremendous challenges to ensure system stability. Few of the challenges include:

- Complex interactions between Operating Systems on heterogeneous SoCs for generic features.
- Lack of centralized knowledge of system state.
- Complex implementation challenges when implementing workarounds for SoC errata.
- Equivalent SoC power or device management entitlement on all variations of Operating Systems.

DMSC controls the power management of the device, hence is responsible for bringing the device out of reset, enforce clock and reset rules. DMSC power management functions are critical to bring device to low power modes, for example DeepSleep, and sense wake-up events to bring device back online to active state. There is one instance of DMSC in this family of devices - WKUP_DMSC0.

Texas Instruments' System Control Interface defines the communication protocol between various processing entities to the System Control Entity on TI SoCs. This is a set of message formats and sequence of operations required to communicate and get system services processed from System Control entity in the SoC.

More information regarding the TI-SCI is given [here](http://processors.wiki.ti.com/index.php/TISCI)¹.

The SCIClient is an interface to the TI-SCI protocol for RTOS and non-OS based applications. It exposes the core message details, valid module/clock IDs to the higher level software and abstracts the communication with the firmware based on the TI-SCI protocol. These APIs can be called by power, resource and security RTOS drivers or any other non-OS or RTOS based higher level software to be able to communicate with DMSC for its services. The higher level software is expected to populate the necessary message core parameters. The SCIClient would wrap the core message with the necessary protocol header and forward this to the DMSC. The SCIClient relies on the CSL-FL layer to program and interact with the Secure Proxy Threads. The SCIClient's goal is to ensure there is no duplication of the interface to the DMSC from different software components which need to interact with the DMSC or other System Control Entities in future devices.

¹ <http://processors.wiki.ti.com/index.php/TISCI>

1.2 Text Conventions

style/bullet	definition or explanation
•	This bullet indicates important information. Please read such text carefully.
•	This bullet indicates additional information.

1.3 Terms and Abbreviation

term	definition or explanation
DMSC	Device Management and Security Controller
SCI	System Control Interface
SYSFW	System Firmware
RA	Ring accelerator
PM	Power Management
RM	Resource Management

1.4 References

1.	TISCI wiki	http://processors.wiki.ti.com/index.php/TISCI
2.	SYSFW confluence page	https://confluence.itg.ti.com/display/SYSFW
3.	DMSC PRD	https://pds.design.ti.com/cgi-bin/showdocumentversions?docid=13286
4.	Secure proxy	https://pds.design.ti.com/d/21/2180/11085/12434/14/ksdma_proxy_1p0p17.doc
5.	RA	https://pds.design.ti.com/d/21/2180/11758/13137/13/ksdma_ringacc_1p0p12.doc

REQUIREMENTS

Requirements at <https://confluence.itg.ti.com/display/Drivers/SciClient+Granular+Requirements> .

2.1 Assumptions

1. The higher level software will populate the core message payload based on the message headers which will be exposed by the SCIClient. The higher level software should include these headers and would populate the core message and send this to the SCIClient.
2. The current implementation of the SCIClient is assumed to be blocking. Until decided later the SCIClient APIs will wait for a completion response from the DMSC firmware on completion of processing before exiting. The API will allow for context switch to other tasks while it waits for the service to complete. In the non-OS case this will be a spinlock.

2.2 Constraints

The host can have multiple outstanding messages to the DMSC firmware. In order to keep track of what messages were being sent out we use the message count and an array to read back the response corresponding to the particular message count. This is especially important when interrupts are being used to understand if the message being received corresponds to the message that we sent. The array size is chosen to be a maximum of how many messages the core can possibly sent out based on the thread ID allocation from DMSC firmware. This may not be optimal for all cores for DDR less systems but is exposed through a macro which if required the user can optimize and re-build the library for. Static allocation is considered for the array hence the macro.

DESIGN DESCRIPTION

The SCIClient has two major functions:

1. Interact with DMSC ROM and load the DMSC Firmware.
2. Pass on service requests from higher level software to the DMSC firmware and forward the response from DMSC firmware to the higher level software.

The *Sciclient_loadfirmware* API is used to cater to the first requirement and the *Sciclient_service* is used to cater to the second. The SCIClient library requires initialization of the a handle which is used by the subsequent API calls. This handle is allocated by the higher level software and is initialized by the [Sciclient_init] function. Once the application/higher level software is being torn down or exiting the *Sciclient_deinit* can be used to de-initialize this handle.

The SCIClient can operate in the following combinations:

1. Non-OS, Polling based message completion.
2. Non-OS, Interrupt Based message completion.
3. RTOS, Polling based message completion.
4. RTOS, Interrupt based message completion.

The SCIClient depends on the PDK OSAL layer to differentiate between the Non-OS and the RTOS implementation of Semaphores and Interrupts (HWIs). The build parameter of the OSAL library would determine if the application is bare metal or RTOS based. The polling versus interrupt based wait for message completion is a run time configuration passed during the SCIClient_init initialization.

All the APIs for interacting with the firmware are blocking with a specified timeout . A common API *Sciclient_service* is implemented for all types of calls to the firmware which takes 3 arguments :

1. **pHandle**
2. **pInPrm**
3. **pOutPrm**

The API serves a particular request, based on the value of messageType parameter in **pInPrms**, whose response is given to the higher level API through **pOutPrms** . The **pInPrms** contains the required inputs from the higher level software corresponding to the message_type, timeout value and the core message as a byte stream. A pointer **pOutPrms** has to be passed to the sciclient ,which shall be modified by sciclient.

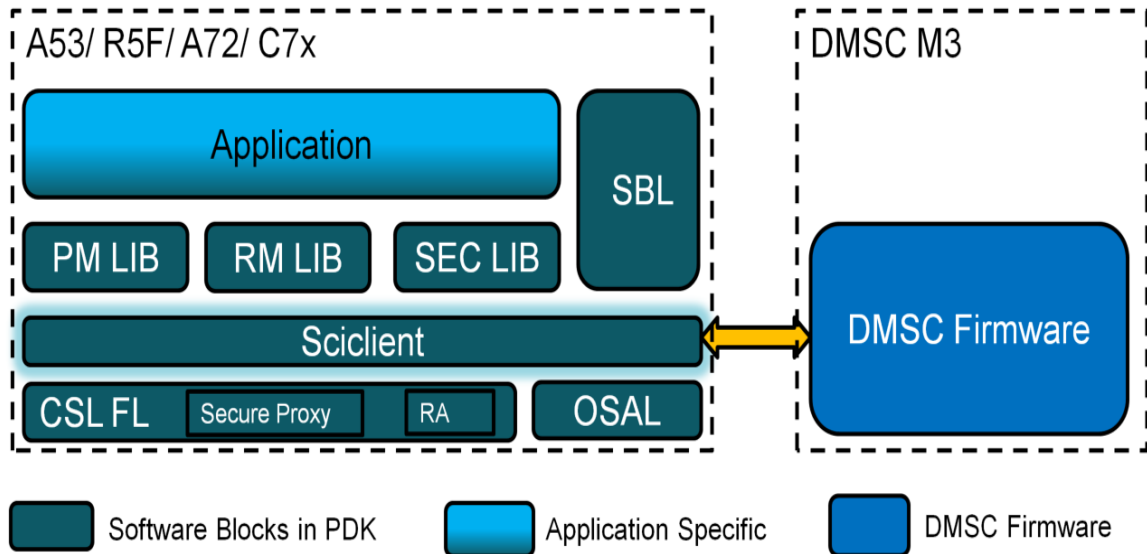
The Sciclient shall be responsible for abstracting all interaction with proxy and RA .

Please refer TISCI² for details of message manager protocol which is used for the requests and responses.

² <http://processors.wiki.ti.com/index.php/TISCI>

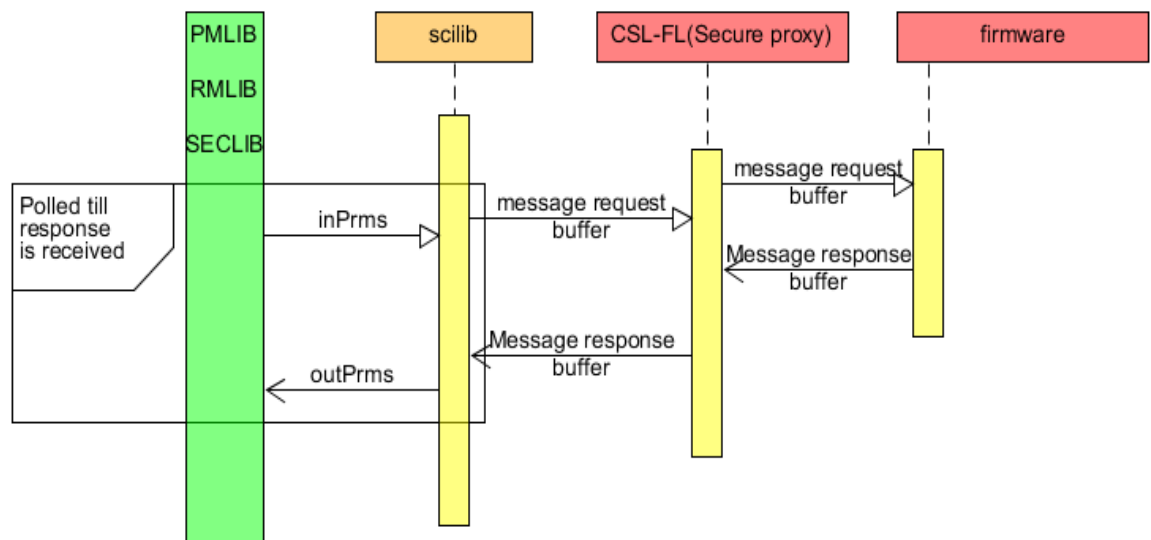
3.1 Component Interaction

Scicient interacts with CSL-FL modules, secure proxy and RA, to interact with the DMSC firmware . Higher level libraries like PM LIB , RM LIB and SECURITY LIB will use Scicient_service API for interaction and will be responsible for filling the core buffer of the request.



3.2 Dynamic behaviour

The high level sequence of operations and its interaction with over components of the Scicient_service API is described in fig.2:



Key Steps of the [Scicient_service] API are:

3.2.1 Construct Message

The message(header+payload) is constructed in normal memory instead of secure proxy memory .

- Find hostId . Refer section 2.2 of [SYSFW](#)³ for hostIds .
- Populate header flags(current support only for TI_SCI_FLAG_REQ_ACK_ON_PROCESSED) and create Message Header. For details on parameters in header, refer [TISCI](#)⁴.
- Append payload to header.

3.2.2 Identify Secure Proxy threads

- Select proxy thread for Tx and Rx based on the pHandle->map . Here, pHandle is a pointer of type ([Sciclient_ServiceHandle_t] *) initialized by [Sciclient_init](#) .

3.2.3 Send Message

- Wait for binary semaphore pHandle->proxySem . Refer [Sciclient_ServiceHandle_t] for definition of proxySem .
- (pHandle->currSeqId++)%[SCICLIENT_MAX_QUEUE_SIZE] . This is for differentiating different [Sciclient_service] calls.
- seqId = pHandle->currSeqId .
- Wait till queue has space till timeout (THREAD[a]_STATUS.curr_cnt > 0)
- initialCount = Rx thread message count .
- Write to Tx thread via secure proxy CSL-FL(CSL_secProxyAccessTarget) .
- Release semaphore pHandle->proxySem.

3.2.4 Wait for response

Sciclient waits for response when *flags* parameter in [Sciclient_ServiceInPrm_t] is TI_SCI_FLAG_REQ_ACK_ON_PROCESSED. Depending on the value of *opModeFlag* parameter in [Sciclient_ServiceHandle_t], there may be polling based or interrupt based execution . A global pointer *gSciclientHandle* = *pHandle* is also maintained for ISR .

opModeFlag=0, Polling	pHandle->opModeFlag=1, Interrupt based
<pre>isMsgReceived = 0; do { Rx count = Rx thread message count if (Rx count > initialCount) { Peek into Rx thread; if(sequenceId received == se- quenceId sent) { isMsgRe- ceived=1; Read full mes- sage to pHandle- >respMsgArr; } } while(!isMsgReceived)</pre>	<pre>retVal=SemaphoreP_pend(pHandle->semSeqId[seqId], pInPrm->timeOut); ISR: {Peek for message SeqId gSciclientHandle- >respMsgArr[seqId] = Read Mes- sage SemaphoreP_post(gSciclientHandle- >semSeqId[SeqId]) }</pre>

³ <https://bitbucket.itg.ti.com/projects/SYSFW/repos/system-firmware/attachments/506ec01f0e/refman-public.pdf>

⁴ http://processors.wiki.ti.com/index.php/TISCI#Generic_Messaging_Header

3.2.5 Construct outPrms

- Extract response header to construct **outPrm** structure
- Copy payload from `pHandle->respMsgArr[pHandle->currSeqId]` to `pOutPayload`.

3.3 Resource Consumption

Sciclient uses the following resources:

- A global pointer *gSciclientHandle* is allocated for ISR. Refer [Sciclient_ServiceHandle_t] .
- A structure for secure proxy base addresses *gSciclient_secProxyCfg* is defined.
- The linker command file for an application using the lib must allocate a section *boardcfg_data* in OC-MSRAM for the default board configuration data .

LOW LEVEL DEFINITIONS

4.1 Constants and Enumerations

4.1.1 Sciclient_ServiceOperationMode

@ { Sciclient Service API Operation Mode. The different types of modes supported are:n (1) Polled Mode : no interrupts are registered. The completion of a message is via polling on the Proxy registers.n (2) Interrupt Mode : Interrupt are registered and the response message would be via a interrupt routine. Default mode in case #Sciclient_ConfigPrms_t is NULL is polled.

Definitions

```
#define SCICLIENT_SERVICE_OPERATION_MODE_POLLED (0U)
#define SCICLIENT_SERVICE_OPERATION_MODE_INTERRUPT (1U)
```

Comments None

Constraints None

See Also None

4.1.2 Sciclient_ServiceOperationTimeout

@ { Sciclient Service API Timeout Values. The different types are:n (1) Wait forever for an operation to complete. n (2) Do not wait for the operation to complete. n (3) Wait for a given time interface for the operation to complete.

Definitions

```
#define SCICLIENT_SERVICE_WAIT_FOREVER (0xFFFFFFFFFU)
#define SCICLIENT_SERVICE_NO_WAIT (0x0U)
```

4.1.3 TISCI_PARAM_UNDEF

Undefined Param Undefined

Definition

```
#define TISCI_PARAM_UNDEF (0xFFFFFFFFFU)
```

Comments None

Constraints None

See Also None

4.1.4 SCICLIENT_FIRMWARE_ABI_MAJOR

ABI Major revision - Major revision changes

- indicate backward compatibility breakage

Definition

```
#define SCICLIENT_FIRMWARE_ABI_MAJOR (2U)
```

Comments None

Constraints None

See Also None

4.1.5 SCICLIENT_FIRMWARE_ABI_MINOR

ABI Minor revision - Minor revision changes

- indicate backward compatibility is maintained,
- however, new messages OR extensions to existing
- messages might have been adde

Definition

```
#define SCICLIENT_FIRMWARE_ABI_MINOR (4U)
```

Comments None

Constraints None

See Also None

4.1.6 SCICLIENT_CONTEXT_R5_NONSEC_0

r5 (Non Secure) : Cortex R5 Context 0 on MCU island

Definition

```
#define SCICLIENT_CONTEXT_R5_NONSEC_0 (0U)
```

Comments None

Constraints None

See Also None

4.1.7 SCICLIENT_CONTEXT_R5_SEC_0

r5 (Secure) : Cortex R5 Context 1 on MCU island (Boot)

Definition

```
#define SCICLIENT_CONTEXT_R5_SEC_0 (1U)
```

Comments None

Constraints None

See Also None

4.1.8 SCICLIENT_CONTEXT_R5_NONSEC_1

r5 (Non Secure) : Cortex R5 Context 2 on MCU island

Definition

```
#define SCICLIENT_CONTEXT_R5_NONSEC_1 (2U)
```

Comments None

Constraints None

See Also None

4.1.9 SCICLIENT_CONTEXT_R5_SEC_1

r5 (Secure) : Cortex R5 Context 3 on MCU island

Definition

```
#define SCICLIENT_CONTEXT_R5_SEC_1 (3U)
```

Comments None

Constraints None

See Also None

4.1.10 SCICLIENT_CONTEXT_A53_SEC_0

a53 (Secure) : Cortex A53 context 0 on Main island

Definition

```
#define SCICLIENT_CONTEXT_A53_SEC_0 (4U)
```

Comments None

Constraints None

See Also None

4.1.11 SCICLIENT_CONTEXT_A53_SEC_1

a53 (Secure) : Cortex A53 context 1 on Main island

Definition

```
#define SCICLIENT_CONTEXT_A53_SEC_1 (5U)
```

Comments None

Constraints None

See Also None

4.1.12 SCICLIENT_CONTEXT_A53_NONSEC_0

a53 (Non Secure) : Cortex A53 context 2 on Main island

Definition

```
#define SCICLIENT_CONTEXT_A53_NONSEC_0 (6U)
```

Comments None

Constraints None

See Also None

4.1.13 SCICLIENT_CONTEXT_A53_NONSEC_1

a53 (Non Secure) : Cortex A53 context 3 on Main island

Definition

```
#define SCICLIENT_CONTEXT_A53_NONSEC_1 (7U)
```

Comments None

Constraints None

See Also None

4.1.14 SCICLIENT_CONTEXT_A53_NONSEC_2

a53 (Non Secure) : Cortex A53 context 4 on Main island

Definition

```
#define SCICLIENT_CONTEXT_A53_NONSEC_2 (8U)
```

Comments None

Constraints None

See Also None

4.1.15 SCICLIENT_CONTEXT_A53_NONSEC_3

a53 (Non Secure) : Cortex A53 context 5 on Main island

Definition

```
#define SCICLIENT_CONTEXT_A53_NONSEC_3 (9U)
```

Comments None

Constraints None

See Also None

4.1.16 SCICLIENT_CONTEXT_A53_NONSEC_4

a53 (Non Secure) : Cortex A53 context 6 on Main island

Definition

```
#define SCICLIENT_CONTEXT_A53_NONSEC_4 (10U)
```

Comments None

Constraints None

See Also None

4.1.17 SCICLIENT_CONTEXT_A53_NONSEC_5

a53 (Non Secure) : Cortex A53 context 7 on Main island

Definition

```
#define SCICLIENT_CONTEXT_A53_NONSEC_5 (11U)
```

Comments None

Constraints None

See Also None

4.1.18 SCICLIENT_CONTEXT_GPU_NONSEC_0

gpu (Non Secure) : SGX544 Context 0 on Main island

Definition

```
#define SCICLIENT_CONTEXT_GPU_NONSEC_0 (12U)
```

Comments None

Constraints None

See Also None

4.1.19 SCICLIENT_CONTEXT_GPU_NONSEC_1

gpu (Non Secure) : SGX544 Context 1 on Main island

Definition

```
#define SCICLIENT_CONTEXT_GPU_NONSEC_1 (13U)
```

Comments None

Constraints None

See Also None

4.1.20 SCICLIENT_CONTEXT_ICSSG_NONSEC_0

icssg (Non Secure) : ICSS Context 0 on Main island

Definition

```
#define SCICLIENT_CONTEXT_ICSSG_NONSEC_0 (14U)
```

Comments None

Constraints None

See Also None

4.1.21 SCICLIENT_CONTEXT_ICSSG_NONSEC_1

icssg (Non Secure) : ICSS Context 1 on Main island

Definition

```
#define SCICLIENT_CONTEXT_ICSSG_NONSEC_1 (15U)
```

Comments None

Constraints None

See Also None

4.1.22 SCICLIENT_CONTEXT_ICSSG_NONSEC_2

icssg (Non Secure) : ICSS Context 2 on Main island

Definition

```
#define SCICLIENT_CONTEXT_ICSSG_NONSEC_2 (16U)
```

Comments None

Constraints None

See Also None

4.1.23 SCICLIENT_CONTEXT_MAX_NUM

Total number of possible contexts for application.

Definition

```
#define SCICLIENT_CONTEXT_MAX_NUM (17U)
```

Comments None

Constraints None

See Also None

4.1.24 Sciclient_PmDeviceIds

@ { Power Management Module Device IDs

Definitions

```
#define TISCI_DEV_MCU_ADC0 (0U)
#define TISCI_DEV_MCU_ADC1 (1U)
#define TISCI_DEV_CAL0 (2U)
#define TISCI_DEV_CMPEVENT_INTRTR0 (3U)
#define TISCI_DEV_MCU_CPSW0 (5U)
#define TISCI_DEV_CPT2_AGGR0 (6U)
#define TISCI_DEV_MCU_CPT2_AGGR0 (7U)
#define TISCI_DEV_STM0 (8U)
#define TISCI_DEV_DCC0 (9U)
#define TISCI_DEV_DCC1 (10U)
#define TISCI_DEV_DCC2 (11U)
#define TISCI_DEV_DCC3 (12U)
#define TISCI_DEV_DCC4 (13U)
#define TISCI_DEV_DCC5 (14U)
```



```
#define TISCI_DEV_DCC6 (15U)
#define TISCI_DEV_DCC7 (16U)
#define TISCI_DEV_MCU_DCC0 (17U)
#define TISCI_DEV_MCU_DCC1 (18U)
#define TISCI_DEV_MCU_DCC2 (19U)
#define TISCI_DEV_DDRSS0 (20U)
#define TISCI_DEV_DEBUGSS_WRAP0 (21U)
#define TISCI_DEV_WKUP_DMSC0 (22U)
#define TISCI_DEV_TIMER0 (23U)
#define TISCI_DEV_TIMER1 (24U)
#define TISCI_DEV_TIMER10 (25U)
#define TISCI_DEV_TIMER11 (26U)
#define TISCI_DEV_TIMER2 (27U)
#define TISCI_DEV_TIMER3 (28U)
#define TISCI_DEV_TIMER4 (29U)
#define TISCI_DEV_TIMER5 (30U)
#define TISCI_DEV_TIMER6 (31U)
#define TISCI_DEV_TIMER7 (32U)
#define TISCI_DEV_TIMER8 (33U)
#define TISCI_DEV_TIMER9 (34U)
#define TISCI_DEV_MCU_TIMER0 (35U)
#define TISCI_DEV_MCU_TIMER1 (36U)
#define TISCI_DEV_MCU_TIMER2 (37U)
#define TISCI_DEV_MCU_TIMER3 (38U)
#define TISCI_DEV_ECAP0 (39U)
#define TISCI_DEV_EHRPWM0 (40U)
#define TISCI_DEV_EHRPWM1 (41U)
#define TISCI_DEV_EHRPWM2 (42U)
#define TISCI_DEV_EHRPWM3 (43U)
#define TISCI_DEV_EHRPWM4 (44U)
#define TISCI_DEV_EHRPWM5 (45U)
#define TISCI_DEV_ELM0 (46U)
#define TISCI_DEV_MMCS0 (47U)
#define TISCI_DEV_MMCS1 (48U)
#define TISCI_DEV_EQEP0 (49U)
#define TISCI_DEV_EQEP1 (50U)
#define TISCI_DEV_EQEP2 (51U)
#define TISCI_DEV_ESM0 (52U)
```

```
#define TISCI_DEV_MCU_ESM0 (53U)
#define TISCI_DEV_WKUP_ESM0 (54U)
#define TISCI_DEV_MCU_FSS0 (55U)
#define TISCI_DEV_GIC0 (56U)
#define TISCI_DEV_GPIO0 (57U)
#define TISCI_DEV_GPIO1 (58U)
#define TISCI_DEV_WKUP_GPIO0 (59U)
#define TISCI_DEV_GPMC0 (60U)
#define TISCI_DEV_GTC0 (61U)
#define TISCI_DEV_PRU_ICSSG0 (62U)
#define TISCI_DEV_PRU_ICSSG1 (63U)
#define TISCI_DEV_PRU_ICSSG2 (64U)
#define TISCI_DEV_GPU0 (65U)
#define TISCI_DEV_CCDEBUGSS0 (66U)
#define TISCI_DEV_DSS0 (67U)
#define TISCI_DEV_DEBUGSS0 (68U)
#define TISCI_DEV_EFUSE0 (69U)
#define TISCI_DEV_PSC0 (70U)
#define TISCI_DEV_MCU_DEBUGSS0 (71U)
#define TISCI_DEV_MCU_EFUSE0 (72U)
#define TISCI_DEV_PBIST0 (73U)
#define TISCI_DEV_PBIST1 (74U)
#define TISCI_DEV_MCU_PBIST0 (75U)
#define TISCI_DEV_PLLCTRL0 (76U)
#define TISCI_DEV_WKUP_PLLCTRL0 (77U)
#define TISCI_DEV_MCU_ROM0 (78U)
#define TISCI_DEV_WKUP_PSC0 (79U)
#define TISCI_DEV_WKUP_VTM0 (80U)
#define TISCI_DEV_DEBUGSUSPENDRTR0 (81U)
#define TISCI_DEV_CBASS0 (82U)
#define TISCI_DEV_CBASS_DEBUG0 (83U)
#define TISCI_DEV_CBASS_FW0 (84U)
#define TISCI_DEV_CBASS_INFRA0 (85U)
#define TISCI_DEV_ECC_AGGR0 (86U)
#define TISCI_DEV_ECC_AGGR1 (87U)
#define TISCI_DEV_ECC_AGGR2 (88U)
#define TISCI_DEV_MCU_CBASS0 (89U)
#define TISCI_DEV_MCU_CBASS_DEBUG0 (90U)
```

```
#define TISCI_DEV_MCU_CBASS_FW0 (91U)
#define TISCI_DEV_MCU_ECC_AGGR0 (92U)
#define TISCI_DEV_MCU_ECC_AGGR1 (93U)
#define TISCI_DEV_WKUP_CBASS0 (94U)
#define TISCI_DEV_WKUP_ECC_AGGR0 (95U)
#define TISCI_DEV_WKUP_CBASS_FW0 (96U)
#define TISCI_DEV_MAIN2MCU_LVL_INTRTR0 (97U)
#define TISCI_DEV_MAIN2MCU_PLS_INTRTR0 (98U)
#define TISCI_DEV_CTRL_MMR0 (99U)
#define TISCI_DEV_GPIOMUX_INTRTR0 (100U)
#define TISCI_DEV_PLL_MMR0 (101U)
#define TISCI_DEV_MCU_MCAN0 (102U)
#define TISCI_DEV_MCU_MCAN1 (103U)
#define TISCI_DEV_MCASP0 (104U)
#define TISCI_DEV_MCASP1 (105U)
#define TISCI_DEV_MCASP2 (106U)
#define TISCI_DEV_MCU_CTRL_MMR0 (107U)
#define TISCI_DEV_MCU_PLL_MMR0 (108U)
#define TISCI_DEV_MCU_SEC_MMR0 (109U)
#define TISCI_DEV_I2C0 (110U)
#define TISCI_DEV_I2C1 (111U)
#define TISCI_DEV_I2C2 (112U)
#define TISCI_DEV_I2C3 (113U)
#define TISCI_DEV_MCU_I2C0 (114U)
#define TISCI_DEV_WKUP_I2C0 (115U)
#define TISCI_DEV_MCU_MSRAM0 (116U)
#define TISCI_DEV_DFTSS0 (117U)
#define TISCI_DEV_NAVSS0 (118U)
#define TISCI_DEV_MCU_NAVSS0 (119U)
#define TISCI_DEV_PCIE0 (120U)
#define TISCI_DEV_PCIE1 (121U)
#define TISCI_DEV_PDMA_DEBUG0 (122U)
#define TISCI_DEV_PDMA0 (123U)
#define TISCI_DEV_PDMA1 (124U)
#define TISCI_DEV_MCU_PDMA0 (125U)
#define TISCI_DEV_MCU_PDMA1 (126U)
#define TISCI_DEV_MCU_PSRAM0 (127U)
#define TISCI_DEV_PSRAMECC0 (128U)
```

```
#define TISCI_DEV_MCU_ARMSS0 (129U)
#define TISCI_DEV_RTI0 (130U)
#define TISCI_DEV_RTI1 (131U)
#define TISCI_DEV_RTI2 (132U)
#define TISCI_DEV_RTI3 (133U)
#define TISCI_DEV_MCU_RTI0 (134U)
#define TISCI_DEV_MCU_RTI1 (135U)
#define TISCI_DEV_SA2_UL0 (136U)
#define TISCI_DEV_MCSPi0 (137U)
#define TISCI_DEV_MCSPi1 (138U)
#define TISCI_DEV_MCSPi2 (139U)
#define TISCI_DEV_MCSPi3 (140U)
#define TISCI_DEV_MCSPi4 (141U)
#define TISCI_DEV_MCU_MCSPi0 (142U)
#define TISCI_DEV_MCU_MCSPi1 (143U)
#define TISCI_DEV_MCU_MCSPi2 (144U)
#define TISCI_DEV_TIMESYNC_INTRTR0 (145U)
#define TISCI_DEV_UART0 (146U)
#define TISCI_DEV_UART1 (147U)
#define TISCI_DEV_UART2 (148U)
#define TISCI_DEV_MCU_UART0 (149U)
#define TISCI_DEV_WKUP_UART0 (150U)
#define TISCI_DEV_USB3SS0 (151U)
#define TISCI_DEV_USB3SS1 (152U)
#define TISCI_DEV_SERDES0 (153U)
#define TISCI_DEV_SERDES1 (154U)
#define TISCI_DEV_WKUP_CTRL_MMR0 (155U)
#define TISCI_DEV_WKUP_GPIOMUX_INTRTR0 (156U)
#define TISCI_DEV_BOARD0 (157U)
#define TISCI_DEV_MCU_ARMSS0_CPU0 (159U)
#define TISCI_DEV_MCU_ARMSS0_COMMON (160U)
#define TISCI_DEV_WKUP_DMSC0_CORTEX_M3_0 (161U)
#define TISCI_DEV_WKUP_DMSC0_INTR_AGGR_0 (162U)
#define TISCI_DEV_NAVSS0_CPTS0 (163U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER0 (164U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER1 (165U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER2 (166U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER3 (167U)
```

```
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER4 (168U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER5 (169U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER6 (170U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER7 (171U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER8 (172U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER9 (173U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER10 (174U)
#define TISCI_DEV_NAVSS0_MAILBOX0_CLUSTER11 (175U)
#define TISCI_DEV_NAVSS0_MCRC0 (176U)
#define TISCI_DEV_NAVSS0_PVU0 (177U)
#define TISCI_DEV_NAVSS0_PVU1 (178U)
#define TISCI_DEV_NAVSS0_UDMASS_INTA0 (179U)
#define TISCI_DEV_NAVSS0_MODSS_INTA0 (180U)
#define TISCI_DEV_NAVSS0_MODSS_INTA1 (181U)
#define TISCI_DEV_NAVSS0_INTR_ROUTER_0 (182U)
#define TISCI_DEV_NAVSS0_TIMER_MGR0 (183U)
#define TISCI_DEV_NAVSS0_TIMER_MGR1 (184U)
#define TISCI_DEV_NAVSS0_PROXY0 (185U)
#define TISCI_DEV_NAVSS0_SEC_PROXY0 (186U)
#define TISCI_DEV_NAVSS0_RINGACC0 (187U)
#define TISCI_DEV_NAVSS0_UDMAP0 (188U)
#define TISCI_DEV_MCU_NAVSS0_INTR_AGGR_0 (189U)
#define TISCI_DEV_MCU_NAVSS0_INTR_ROUTER_0 (190U)
#define TISCI_DEV_MCU_NAVSS0_PROXY0 (191U)
#define TISCI_DEV_MCU_NAVSS0_SEC_PROXY0 (192U)
#define TISCI_DEV_MCU_NAVSS0_MCRC0 (193U)
#define TISCI_DEV_MCU_NAVSS0_UDMAP0 (194U)
#define TISCI_DEV_MCU_NAVSS0_RINGACC0 (195U)
#define TISCI_DEV_COMPUTE_CLUSTER_MSMC0 (196U)
#define TISCI_DEV_COMPUTE_CLUSTER_PBIST0 (197U)
#define TISCI_DEV_COMPUTE_CLUSTER_CPAC0 (198U)
#define TISCI_DEV_COMPUTE_CLUSTER_CPAC_PBIST0 (199U)
#define TISCI_DEV_COMPUTE_CLUSTER_CPAC1 (200U)
#define TISCI_DEV_COMPUTE_CLUSTER_CPAC_PBIST1 (201U)
#define TISCI_DEV_COMPUTE_CLUSTER_A53_0 (202U)
#define TISCI_DEV_COMPUTE_CLUSTER_A53_1 (203U)
#define TISCI_DEV_COMPUTE_CLUSTER_A53_2 (204U)
#define TISCI_DEV_COMPUTE_CLUSTER_A53_3 (205U)
```

```

#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVSRAMLO_4 (206U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_FSS_S1_3 (207U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_EXPORT_SLV_0 (208U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVSRAMHI_3 (209U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_SRAM_SLV_1 (210U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVDDRHI_5 (211U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVDDRLO_6 (212U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_CAL0_0 (213U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_DSS_2 (214U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_FSS_S0_2 (215U)
#define TISCI_DEV_OLDI_TX_CORE_MAIN_0 (216U)
#define TISCI_DEV_K3_ARM_ATB_FUNNEL_3_32_MCU_0 (217U)
#define TISCI_DEV_ICEMELTER_WKUP_0 (218U)
#define TISCI_DEV_K3_LED_MAIN_0 (219U)
#define TISCI_DEV_VDC_DATA_VBUSM_32B_REF_WKUP2MCU (220U)
#define TISCI_DEV_VDC_DATA_VBUSM_32B_REF_MCU2WKUP (221U)
#define TISCI_DEV_VDC_DATA_VBUSM_64B_REF_MAIN2MCU (222U)
#define TISCI_DEV_VDC_DATA_VBUSM_64B_REF_MCU2MAIN (223U)
#define TISCI_DEV_VDC_DMSC_DBG_VBUSP_32B_REF_DBG2DMSC (224U)
#define TISCI_DEV_VDC_INFRA_VBUSP_32B_REF_WKUP2MAIN_INFRA (225U)
#define TISCI_DEV_VDC_INFRA_VBUSP_32B_REF_MCU2MAIN_INFRA (226U)
#define TISCI_DEV_VDC_SOC_FW_VBUSP_32B_REF_FWWKUP2MCU (227U)
#define TISCI_DEV_VDC_SOC_FW_VBUSP_32B_REF_FWMCU2MAIN (228U)
#define TISCI_DEV_VDC_MCU_DBG_VBUSP_32B_REF_DBGMAIN2MCU (229U)
#define TISCI_DEV_VDC_NAV_PSIL_128B_REF_MAIN2MCU (230U)
#define TISCI_DEV_GS80PRG_SOC_WRAP_WKUP_0 (231U)
#define TISCI_DEV_GS80PRG_MCU_WRAP_WKUP_0 (232U)
#define TISCI_DEV_MX_WAKEUP_RESET_SYNC_WKUP_0 (233U)
#define TISCI_DEV_MX_EFUSE_MAIN_CHAIN_MAIN_0 (234U)
#define TISCI_DEV_MX_EFUSE_MCU_CHAIN_MCU_0 (235U)
#define TISCI_DEV_DUMMY_IP_LPSC_WKUP2MCU (236U)
#define TISCI_DEV_DUMMY_IP_LPSC_WKUP2MAIN_INFRA (237U)
#define TISCI_DEV_DUMMY_IP_LPSC_DEBUG2DMSC (238U)
#define TISCI_DEV_DUMMY_IP_LPSC_DMSC (239U)
#define TISCI_DEV_DUMMY_IP_LPSC_MCU2MAIN_INFRA (240U)
#define TISCI_DEV_DUMMY_IP_LPSC_MCU2MAIN (241U)
#define TISCI_DEV_DUMMY_IP_LPSC_MCU2WKUP (242U)
#define TISCI_DEV_DUMMY_IP_LPSC_MAIN2MCU (243U)

```

```
#define TISCI_DEV_DUMMY_IP_LPSC_EMIF_DATA (244U)
#define TISCI_DEV_MCU_ARMSS0_CPU1 (245U)
#define TISCI_DEV_MAX (246U)
```

Comments None

Constraints None

See Also None

4.1.25 Sciclient_PmModuleClockIds

@ { Power Management Module Clock IDs for individual modules.

Definitions

```
#define TISCI_DEV_DCC4_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_DCC4_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_DCC4_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_DCC4_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_DCC4_BUS_VBUS_CLK (4U)
#define TISCI_DEV_DCC4_BUS_DCC_INPUT01_CLK (5U)
#define TISCI_DEV_DCC4_BUS_DCC_CLKSRC5_CLK (6U)
#define TISCI_DEV_DCC4_BUS_DCC_INPUT02_CLK (7U)
#define TISCI_DEV_DCC4_BUS_DCC_CLKSRC0_CLK (8U)
#define TISCI_DEV_DCC4_BUS_DCC_CLKSRC6_CLK (9U)
#define TISCI_DEV_DCC4_BUS_DCC_INPUT10_CLK (10U)
#define TISCI_DEV_DCC4_BUS_DCC_CLKSRC2_CLK (11U)
#define TISCI_DEV_DCC6_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_DCC6_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_DCC6_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_DCC6_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_DCC6_BUS_VBUS_CLK (4U)
#define TISCI_DEV_DCC6_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_DCC6_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_DCC6_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_DCC6_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_DCC6_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_DCC6_BUS_DCC_CLKSRC6_CLK (10U)
#define TISCI_DEV_DCC6_BUS_DCC_INPUT10_CLK (11U)
#define TISCI_DEV_DCC6_BUS_DCC_CLKSRC2_CLK (12U)
#define TISCI_DEV_DCC0_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_DCC0_BUS_DCC_CLKSRC4_CLK (1U)
#define TISCI_DEV_DCC0_BUS_DCC_CLKSRC3_CLK (2U)
```

```

#define TISCI_DEV_DCC0_BUS_VBUS_CLK (3U)
#define TISCI_DEV_DCC0_BUS_DCC_CLKSRC1_CLK (4U)
#define TISCI_DEV_DCC0_BUS_DCC_INPUT01_CLK (5U)
#define TISCI_DEV_DCC0_BUS_DCC_CLKSRC5_CLK (6U)
#define TISCI_DEV_DCC0_BUS_DCC_INPUT02_CLK (7U)
#define TISCI_DEV_DCC0_BUS_DCC_CLKSRC0_CLK (8U)
#define TISCI_DEV_DCC0_BUS_DCC_CLKSRC6_CLK (9U)
#define TISCI_DEV_DCC0_BUS_DCC_INPUT10_CLK (10U)
#define TISCI_DEV_DCC0_BUS_DCC_CLKSRC2_CLK (11U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_MCU_DCC2_BUS_VBUS_CLK (4U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_CLKSRC6_CLK (10U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_INPUT10_CLK (11U)
#define TISCI_DEV_MCU_DCC2_BUS_DCC_CLKSRC2_CLK (12U)
#define TISCI_DEV_DCC5_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_DCC5_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_DCC5_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_DCC5_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_DCC5_BUS_VBUS_CLK (4U)
#define TISCI_DEV_DCC5_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_DCC5_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_DCC5_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_DCC5_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_DCC5_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_DCC5_BUS_DCC_CLKSRC6_CLK (10U)
#define TISCI_DEV_DCC5_BUS_DCC_INPUT10_CLK (11U)
#define TISCI_DEV_DCC5_BUS_DCC_CLKSRC2_CLK (12U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_CLKSRC4_CLK (2U)

```



```
#define TISCI_DEV_MCU_DCC0_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_MCU_DCC0_BUS_VBUS_CLK (4U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_CLKSRC6_CLK (10U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_INPUT10_CLK (11U)
#define TISCI_DEV_MCU_DCC0_BUS_DCC_CLKSRC2_CLK (12U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_MCU_DCC1_BUS_VBUS_CLK (4U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_CLKSRC6_CLK (10U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_INPUT10_CLK (11U)
#define TISCI_DEV_MCU_DCC1_BUS_DCC_CLKSRC2_CLK (12U)
#define TISCI_DEV_DCC1_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_DCC1_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_DCC1_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_DCC1_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_DCC1_BUS_VBUS_CLK (4U)
#define TISCI_DEV_DCC1_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_DCC1_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_DCC1_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_DCC1_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_DCC1_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_DCC1_BUS_DCC_CLKSRC6_CLK (10U)
#define TISCI_DEV_DCC1_BUS_DCC_INPUT10_CLK (11U)
#define TISCI_DEV_DCC1_BUS_DCC_CLKSRC2_CLK (12U)
#define TISCI_DEV_DCC3_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_DCC3_BUS_DCC_CLKSRC7_CLK (1U)
```

```

#define TISCI_DEV_DCC3_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_DCC3_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_DCC3_BUS_VBUS_CLK (4U)
#define TISCI_DEV_DCC3_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_DCC3_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_DCC3_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_DCC3_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_DCC3_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_DCC3_BUS_DCC_INPUT10_CLK (10U)
#define TISCI_DEV_DCC3_BUS_DCC_CLKSRC2_CLK (11U)
#define TISCI_DEV_DCC7_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_DCC7_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_DCC7_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_DCC7_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_DCC7_BUS_VBUS_CLK (4U)
#define TISCI_DEV_DCC7_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_DCC7_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_DCC7_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_DCC7_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_DCC7_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_DCC7_BUS_DCC_CLKSRC6_CLK (10U)
#define TISCI_DEV_DCC7_BUS_DCC_INPUT10_CLK (11U)
#define TISCI_DEV_DCC7_BUS_DCC_CLKSRC2_CLK (12U)
#define TISCI_DEV_DCC2_BUS_DCC_INPUT00_CLK (0U)
#define TISCI_DEV_DCC2_BUS_DCC_CLKSRC7_CLK (1U)
#define TISCI_DEV_DCC2_BUS_DCC_CLKSRC4_CLK (2U)
#define TISCI_DEV_DCC2_BUS_DCC_CLKSRC3_CLK (3U)
#define TISCI_DEV_DCC2_BUS_VBUS_CLK (4U)
#define TISCI_DEV_DCC2_BUS_DCC_CLKSRC1_CLK (5U)
#define TISCI_DEV_DCC2_BUS_DCC_INPUT01_CLK (6U)
#define TISCI_DEV_DCC2_BUS_DCC_CLKSRC5_CLK (7U)
#define TISCI_DEV_DCC2_BUS_DCC_INPUT02_CLK (8U)
#define TISCI_DEV_DCC2_BUS_DCC_CLKSRC0_CLK (9U)
#define TISCI_DEV_DCC2_BUS_DCC_CLKSRC6_CLK (10U)
#define TISCI_DEV_DCC2_BUS_DCC_INPUT10_CLK (11U)
#define TISCI_DEV_DCC2_BUS_DCC_CLKSRC2_CLK (12U)
#define TISCI_DEV_MCU_I2C0_BUS_CLK (0U)
#define TISCI_DEV_MCU_I2C0_BUS_PISYS_CLK (1U)

```

```
#define TISCI_DEV_MCU_I2C0_BUS_PISCL (2U)
#define TISCI_DEV_I2C3_BUS_CLK (0U)
#define TISCI_DEV_I2C3_BUS_PISYS_CLK (1U)
#define TISCI_DEV_I2C3_BUS_PISCL (2U)
#define TISCI_DEV_I2C2_BUS_CLK (0U)
#define TISCI_DEV_I2C2_BUS_PISYS_CLK (1U)
#define TISCI_DEV_I2C2_BUS_PISCL (2U)
#define TISCI_DEV_WKUP_I2C0_BUS_CLK (0U)
#define TISCI_DEV_WKUP_I2C0_BUS_PISYS_CLK (1U)
#define TISCI_DEV_WKUP_I2C0_BUS_PISYS_CLK_PARENT_ADPLLH_HSDIV_WRAP_MCU_1_BUS_PISCL (2U)
#define TISCI_DEV_WKUP_I2C0_BUS_PISYS_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_CLK (3U)
#define TISCI_DEV_WKUP_I2C0_BUS_PISCL (4U)
#define TISCI_DEV_I2C0_BUS_CLK (0U)
#define TISCI_DEV_I2C0_BUS_PISYS_CLK (1U)
#define TISCI_DEV_I2C0_BUS_PISCL (2U)
#define TISCI_DEV_I2C1_BUS_CLK (0U)
#define TISCI_DEV_I2C1_BUS_PISYS_CLK (1U)
#define TISCI_DEV_I2C1_BUS_PISCL (2U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_TIMER_TCLK_CLK (1U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK (2U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_ADPLLHJM_HSDIV_WRAP_MAIN_0_TIMER_TCLK_CLK (3U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_TIMER_TCLK_CLK (4U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_ADPLLH_HSDIV_WRAP_MCU_1_BUS_TIMER_TCLK_CLK (5U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK1 (6U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1 (7U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT_TIMER_TCLK_CLK (8U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK (9U)
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_ADPLLHJM_HSDIV_WRAP_MAIN_2_TIMER_TCLK_CLK (10U)
```

```
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_WRAP_MAIN_1_BUS_CI  
(11U)  
#define TISCI_DEV_TIMER5_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS  
(12U)  
#define TISCI_DEV_TIMER5_BUS_TIMER_HCLK_CLK (13U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK (0U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS  
(1U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK  
(2U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0  
(3U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS  
(4U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BU  
(5U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK  
(6U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1  
(7U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT  
(8U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK  
(9U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_2  
(10U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_WRAP_MAIN_1_BUS_CI  
(11U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS  
(12U)  
#define TISCI_DEV_TIMER6_BUS_TIMER_HCLK_CLK (13U)  
#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK (0U)  
#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS  
(1U)  
#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK  
(2U)  
#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0  
(3U)  
#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS  
(4U)  
#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BU  
(5U)  
#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK  
(6U)
```

```
#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)

#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)

#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)

#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJH_HSDIV_WRAP_MAIN_2
(10U)

#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJH_WRAP_MAIN_1_BUS_C
(11U)

#define TISCI_DEV_TIMER7_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(12U)

#define TISCI_DEV_TIMER7_BUS_TIMER_HCLK_CLK (13U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK (0U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(1U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP
(2U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(3U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_ADPLLH_HSDIV_WRAP_MCU
(4U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_R
(5U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS
(6U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_CPSW_2GUSS_MCU_0_BUS_C
(7U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(8U)

#define TISCI_DEV_MCU_TIMER0_BUS_TIMER_HCLK_CLK (9U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK (0U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(1U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJH_HSDIV_WRAP_MAIN_0
(3U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(4U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_ADPLLH_HSDIV_WRAP_MCU_1_B
(5U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)
```

```
#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_2
(10U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_1_BUS_C
(11U)

#define TISCI_DEV_TIMER8_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(12U)

#define TISCI_DEV_TIMER8_BUS_TIMER_HCLK_CLK (13U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK (0U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(1U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_0
(3U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(4U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MCU_1_BU
(5U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_2
(10U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_1_BUS_C
(11U)

#define TISCI_DEV_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(12U)

#define TISCI_DEV_TIMER2_BUS_TIMER_HCLK_CLK (13U)

#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK (0U)

#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(1U)

#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP
(2U)
```

```
#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(3U)
#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(4U)
#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_R
(5U)
#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_B
(6U)
#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_CPSW_2GUSS_MCU_0_B
(7U)
#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(8U)
#define TISCI_DEV_MCU_TIMER1_BUS_TIMER_HCLK_CLK (9U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(1U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP
(2U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(3U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(4U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_R
(5U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_B
(6U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_CPSW_2GUSS_MCU_0_B
(7U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(8U)
#define TISCI_DEV_MCU_TIMER2_BUS_TIMER_HCLK_CLK (9U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_B
(1U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0
(3U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_B
(4U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_B
(5U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)
```

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#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_2
(10U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_1_BUS_C
(11U)
#define TISCI_DEV_TIMER4_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(12U)
#define TISCI_DEV_TIMER4_BUS_TIMER_HCLK_CLK (13U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(1U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_0
(3U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(4U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MCU_1_BU
(5U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_2
(10U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJMHSDIV_WRAP_MAIN_1_BUS_C
(11U)
#define TISCI_DEV_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(12U)
#define TISCI_DEV_TIMER3_BUS_TIMER_HCLK_CLK (13U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(1U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)

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#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_
(3U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_
(4U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_B
(5U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_2_
(10U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_WRAP_MAIN_1_BUS_C
(11U)
#define TISCI_DEV_TIMER9_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_
(12U)
#define TISCI_DEV_TIMER9_BUS_TIMER_HCLK_CLK (13U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_
(1U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_
(3U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_
(4U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_B
(5U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_2_
(10U)
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_WRAP_MAIN_1_BUS_C
(11U)
```

```
#define TISCI_DEV_TIMER11_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(12U)
#define TISCI_DEV_TIMER11_BUS_TIMER_HCLK_CLK (13U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(1U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJLM_HSDIV_WRAP_MAIN_0
(3U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(4U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJLM_HSDIV_WRAP_MCU_1_B
(5U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OU
(8U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJLM_HSDIV_WRAP_MAIN_2
(10U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJLM_WRAP_MAIN_1_BUS_C
(11U)
#define TISCI_DEV_TIMER10_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(12U)
#define TISCI_DEV_TIMER10_BUS_TIMER_HCLK_CLK (13U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(1U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJLM_HSDIV_WRAP_MAIN_0
(3U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(4U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_ADPLLJLM_HSDIV_WRAP_MCU_1_B
(5U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)
```

```
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_2
(10U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_WRAP_MAIN_1_BUS_C
(11U)
#define TISCI_DEV_TIMER0_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(12U)
#define TISCI_DEV_TIMER0_BUS_TIMER_HCLK_CLK (13U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(1U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP
(2U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(3U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(4U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_R
(5U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS
(6U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_CPSW_2GUSS_MCU_0_BUS_C
(7U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0
(8U)
#define TISCI_DEV_MCU_TIMER3_BUS_TIMER_HCLK_CLK (9U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK (0U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(1U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(2U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0
(3U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS
(4U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_B
(5U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK
(6U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(7U)
```

```

#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(8U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(9U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_2_
(10U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_ADPLLLJM_WRAP_MAIN_1_BUS_C
(11U)
#define TISCI_DEV_TIMER1_BUS_TIMER_TCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_
(12U)
#define TISCI_DEV_TIMER1_BUS_TIMER_HCLK_CLK (13U)
#define TISCI_DEV_WKUP_PSC0_BUS_CLK (0U)
#define TISCI_DEV_WKUP_PSC0_BUS_SLOW_CLK (1U)
#define TISCI_DEV_CBASS0_BUS_MAIN_SYSCLK0_2_CLK (0U)
#define TISCI_DEV_CBASS0_BUS_MAIN_SYSCLK0_4_CLK (1U)
#define TISCI_DEV_PLL_MMR0_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_MCU_CPT2_AGGR0_BUS_VCLK_CLK (0U)
#define TISCI_DEV_CPT2_AGGR0_BUS_VCLK_CLK (0U)
#define TISCI_DEV_DEBUGSS0_BUS_ATB1_CLK (0U)
#define TISCI_DEV_DEBUGSS0_BUS_ATB5_CLK (1U)
#define TISCI_DEV_DEBUGSS0_BUS_ATB0_CLK (2U)
#define TISCI_DEV_DEBUGSS0_BUS_SYS_CLK (3U)
#define TISCI_DEV_DEBUGSS0_BUS_ATB4_CLK (4U)
#define TISCI_DEV_DEBUGSS0_BUS_CFG_CLK (5U)
#define TISCI_DEV_DEBUGSS0_BUS_ATB2_CLK (6U)
#define TISCI_DEV_DEBUGSS0_BUS_DBG_CLK (7U)
#define TISCI_DEV_DEBUGSS0_BUS_ATB3_CLK (8U)
#define TISCI_DEV_EHRPWM4_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_EHRPWM1_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_EHRPWM0_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_EHRPWM3_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_EHRPWM5_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_EHRPWM2_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_ELM0_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_MCU_UART0_BUS_FCLK_CLK (0U)
#define TISCI_DEV_MCU_UART0_BUS_FCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_
(1U)
#define TISCI_DEV_MCU_UART0_BUS_FCLK_CLK_PARENT_ADPLLLJM_WRAP_MAIN_1_BUS_CLK
(2U)
#define TISCI_DEV_MCU_UART0_BUS_VBUSP_CLK (3U)

```

```
#define TISCI_DEV_WKUP_UART0_BUS_FCLK_CLK (0U)
#define TISCI_DEV_WKUP_UART0_BUS_FCLK_CLK_PARENT_CLOCKMUX_WKUPUSART_CLK_SEL_
(1U)
#define TISCI_DEV_WKUP_UART0_BUS_FCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_W
(2U)
#define TISCI_DEV_WKUP_UART0_BUS_VBUSEP_CLK (3U)
#define TISCI_DEV_UART1_BUS_FCLK_CLK (0U)
#define TISCI_DEV_UART1_BUS_VBUSEP_CLK (1U)
#define TISCI_DEV_UART0_BUS_FCLK_CLK (0U)
#define TISCI_DEV_UART0_BUS_VBUSEP_CLK (1U)
#define TISCI_DEV_UART2_BUS_FCLK_CLK (0U)
#define TISCI_DEV_UART2_BUS_VBUSEP_CLK (1U)
#define TISCI_DEV_SA2_UL0_BUS_PKA_IN_CLK (0U)
#define TISCI_DEV_SA2_UL0_BUS_X1_CLK (1U)
#define TISCI_DEV_SA2_UL0_BUS_X2_CLK (2U)
#define TISCI_DEV_CAL0_BUS_CLK (0U)
#define TISCI_DEV_CAL0_BUS_CP_C_CLK (1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVSRAMLO_4_BUS_VBUS_CLK
(0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVSRAMLO_4_BUS_PROBE_CLK
(1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_FSS_S1_3_BUS_VBUS_CLK (0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_FSS_S1_3_BUS_PROBE_CLK
(1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_EXPORT_SLV_0_BUS_VBUS_CLK
(0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_EXPORT_SLV_0_BUS_PROBE_CLK
(1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVSRAMHI_3_BUS_VBUS_CLK
(0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVSRAMHI_3_BUS_PROBE_CLK
(1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_SRAM_SLV_1_BUS_VBUS_CLK
(0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_SRAM_SLV_1_BUS_PROBE_CLK
(1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVDDRHI_5_BUS_VBUS_CLK
(0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVDDRHI_5_BUS_PROBE_CLK
(1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVDDRLO_6_BUS_VBUS_CLK
(0U)
```

```

#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_NAVDDRLO_6_BUS_PROBE_CLK
(1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_CAL0_0_BUS_VBUS_CLK (0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_CAL0_0_BUS_PROBE_CLK (1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_DSS_2_BUS_VBUS_CLK (0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MAIN_DSS_2_BUS_PROBE_CLK (1U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_FSS_S0_2_BUS_VBUS_CLK (0U)
#define TISCI_DEV_CPT2_PROBE_VBUSM_MCU_FSS_S0_2_BUS_PROBE_CLK
(1U)
#define TISCI_DEV_PBIST0_BUS_CLK1_CLK (0U)
#define TISCI_DEV_PBIST0_BUS_CLK4_CLK (1U)
#define TISCI_DEV_PBIST0_BUS_CLK2_CLK (2U)
#define TISCI_DEV_PBIST1_BUS_CLK1_CLK (0U)
#define TISCI_DEV_PBIST1_BUS_CLK4_CLK (1U)
#define TISCI_DEV_PBIST1_BUS_CLK2_CLK (2U)
#define TISCI_DEV_MCU_PBIST0_BUS_CLK1_CLK (0U)
#define TISCI_DEV_MCU_PBIST0_BUS_CLK4_CLK (1U)
#define TISCI_DEV_MCU_PBIST0_BUS_CLK2_CLK (2U)
#define TISCI_DEV_NAVSS0_BUS_UDMASS_VD2CLK (0U)
#define TISCI_DEV_NAVSS0_BUS_ICSS_G2CLK (1U)
#define TISCI_DEV_NAVSS0_BUS_ICSS_G0CLK (2U)
#define TISCI_DEV_NAVSS0_BUS_RCLK_BUS_IN3_BOARD_0_BUS_CPTS_RFT_CLK
(3U)
#define TISCI_DEV_NAVSS0_BUS_MSMC0CLK (4U)
#define TISCI_DEV_NAVSS0_BUS_RCLK_BUS_IN0_ADPLLM_HSDIV_WRAP_MCU_1_BUS_HSDIV_CLK
(5U)
#define TISCI_DEV_NAVSS0_BUS_RCLK_BUS_IN2_BOARD_0_BUS_MCU_CPTS_RFT_CLK
(6U)
#define TISCI_DEV_NAVSS0_BUS_MODSS_VD2CLK (7U)
#define TISCI_DEV_NAVSS0_BUS_RCLK_BUS_IN4_BOARD_0_BUS_MCU_EXT_REFCLK0
(8U)
#define TISCI_DEV_NAVSS0_BUS_PDMA_MAIN1CLK (9U)
#define TISCI_DEV_NAVSS0_BUS_NBSS_VCLK (10U)
#define TISCI_DEV_NAVSS0_BUS_RCLK_BUS_IN1_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_HSDIV_
(11U)
#define TISCI_DEV_NAVSS0_BUS_NBSS_VD2CLK (12U)
#define TISCI_DEV_NAVSS0_BUS_ICSS_G1CLK (13U)
#define TISCI_DEV_NAVSS0_BUS_RCLK_BUS_IN5_BOARD_0_BUS_EXT_REFCLK1
(14U)
#define TISCI_DEV_DSS0_BUS_DPI_0_IN_CLK_BUS_IN1_CLOCKDIVIDER_DSS_BUS_OUT0
(0U)

```

```
#define TISCI_DEV_DSS0_BUS_DSS_FUNC_CLK (1U)
#define TISCI_DEV_DSS0_BUS_DPI_1_IN_CLK (2U)
#define TISCI_DEV_DSS0_BUS_DPI_1_IN_CLK_PARENT_CLOCKDIVIDER_DSS_BUS_OUT07
(3U)
#define TISCI_DEV_DSS0_BUS_DPI_1_IN_CLK_PARENT_BOARD_0_BUS_DSS0EXTPCLKIN
(4U)
#define TISCI_DEV_DSS0_BUS_DPI_1_IN_CLK_PARENT_CLOCKDIVIDER_DSS_BUS_OUT1
(5U)
#define TISCI_DEV_DSS0_BUS_DPI_0_IN_CLK_BUS_IN0_CLOCKDIVIDER_DSS_BUS_OUT0
(6U)
#define TISCI_DEV_DSS0_BUS_DPI_1_OUT_CLK (7U)
#define TISCI_DEV_GPMC0_BUS_FUNC_CLK (0U)
#define TISCI_DEV_GPMC0_BUS_FUNC_CLK_PARENT_ADPLLH_HSDIV_WRAP_MCU_1_BUS_HSDIV
(1U)
#define TISCI_DEV_GPMC0_BUS_FUNC_CLK_PARENT_ADPLLH_HSDIV_WRAP_MAIN_2_BUS_CL
(2U)
#define TISCI_DEV_GPMC0_BUS_FUNC_CLK_PARENT_ADPLLH_HSDIV_WRAP_MAIN_2_BUS_CL
(3U)
#define TISCI_DEV_GPMC0_BUS_FUNC_CLK_PARENT_K3_PLL_CTRL_WRAP_MAIN_0_BUS_CHIP_
(4U)
#define TISCI_DEV_GPMC0_BUS_PI_GPMC_RET_CLK (5U)
#define TISCI_DEV_GPMC0_BUS_VBUSP_CLK (6U)
#define TISCI_DEV_GPMC0_BUS_PO_GPMC_DEV_CLK (7U)
#define TISCI_DEV_MMCS01_BUS_EMMCSDSS_VBUS_CLK (0U)
#define TISCI_DEV_MMCS01_BUS_EMMCSDSS_XIN_CLK (1U)
#define TISCI_DEV_WKUP_PLLCTRL0_BUS_VBUS_SLV_REFCLK_CLK (0U)
#define TISCI_DEV_WKUP_PLLCTRL0_BUS_PLL_CLKOUT_CLK (1U)
#define TISCI_DEV_WKUP_PLLCTRL0_BUS_PLL_REFCLK_CLK (2U)
#define TISCI_DEV_PLLCTRL0_BUS_VBUS_SLV_REFCLK_CLK (0U)
#define TISCI_DEV_PLLCTRL0_BUS_PLL_CLKOUT_CLK (1U)
#define TISCI_DEV_PLLCTRL0_BUS_PLL_REFCLK_CLK (2U)
#define TISCI_DEV_PLLCTRL0_BUS_PLL_REFCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BU
(3U)
#define TISCI_DEV_PLLCTRL0_BUS_PLL_REFCLK_CLK_PARENT_BOARD_0_HFOSC1_CLK
(4U)
#define TISCI_DEV_USB3SS1_BUS_SUSP_CLK (0U)
#define TISCI_DEV_USB3SS1_BUS_PHY2_REFCLK960M_CLK (1U)
#define TISCI_DEV_USB3SS1_BUS_REF_CLK (2U)
#define TISCI_DEV_USB3SS1_BUS_REF_CLK_PARENT_CLOCKMUX_HFOSC_SEL_BUS_OUT0
(3U)
#define TISCI_DEV_USB3SS1_BUS_REF_CLK_PARENT_ADPLLH_HSDIV_WRAP_MAIN_1_BUS_CLKOUT_C
(4U)
```

```

#define TISCI_DEV_USB3SS1_BUS_HSIC_CLK_CLK (5U)
#define TISCI_DEV_USB3SS1_BUS_BUS_CLK (6U)
#define TISCI_DEV_USB3SS1_BUS_PIPE3_TXB_CLK (7U)
#define TISCI_DEV_USB3SS1_BUS_UTMI_CLK_CLK (8U)
#define TISCI_DEV_USB3SS0_BUS_SUSP_CLK (0U)
#define TISCI_DEV_USB3SS0_BUS_PHY2_REFCLK960M_CLK (1U)
#define TISCI_DEV_USB3SS0_BUS_REF_CLK (2U)
#define TISCI_DEV_USB3SS0_BUS_REF_CLK_PARENT_CLOCKMUX_HFOSC_SEL_BUS_OUT0
(3U)
#define TISCI_DEV_USB3SS0_BUS_REF_CLK_PARENT_ADPLLJMW_WRAP_MAIN_1_BUS_CLKOUT_0
(4U)
#define TISCI_DEV_USB3SS0_BUS_HSIC_CLK_CLK (5U)
#define TISCI_DEV_USB3SS0_BUS_BUS_CLK (6U)
#define TISCI_DEV_USB3SS0_BUS_PIPE3_TXB_CLK (7U)
#define TISCI_DEV_USB3SS0_BUS_PIPE3_TXB_CLK_PARENT_WIZ8B2M4VSB_MAIN_0_BUS_LN0_TX
(8U)
#define TISCI_DEV_USB3SS0_BUS_PIPE3_TXB_CLK_PARENT_CLOCKMUX_USB0_PIPE3_CLK_SEL_1
(9U)
#define TISCI_DEV_USB3SS0_BUS_UTMI_CLK_CLK (10U)
#define TISCI_DEV_MCU_MCSPi0_BUS_IO_CLKSPiI_CLK (0U)
#define TISCI_DEV_MCU_MCSPi0_BUS_CLKSPiREF_CLK (1U)
#define TISCI_DEV_MCU_MCSPi0_BUS_VBUSP_CLK (2U)
#define TISCI_DEV_MCU_MCSPi0_BUS_IO_CLKSPiO_CLK (3U)
#define TISCI_DEV_MCSPi2_BUS_IO_CLKSPiI_CLK (0U)
#define TISCI_DEV_MCSPi2_BUS_CLKSPiREF_CLK (1U)
#define TISCI_DEV_MCSPi2_BUS_VBUSP_CLK (2U)
#define TISCI_DEV_MCSPi2_BUS_IO_CLKSPiO_CLK (3U)
#define TISCI_DEV_MCU_MCSPi2_BUS_CLKSPiREF_CLK (0U)
#define TISCI_DEV_MCU_MCSPi2_BUS_VBUSP_CLK (1U)
#define TISCI_DEV_MCSPi0_BUS_IO_CLKSPiI_CLK (0U)
#define TISCI_DEV_MCSPi0_BUS_CLKSPiREF_CLK (1U)
#define TISCI_DEV_MCSPi0_BUS_VBUSP_CLK (2U)
#define TISCI_DEV_MCSPi0_BUS_IO_CLKSPiO_CLK (3U)
#define TISCI_DEV_MCSPi1_BUS_IO_CLKSPiI_CLK (0U)
#define TISCI_DEV_MCSPi1_BUS_CLKSPiREF_CLK (1U)
#define TISCI_DEV_MCSPi1_BUS_VBUSP_CLK (2U)
#define TISCI_DEV_MCSPi1_BUS_IO_CLKSPiO_CLK (3U)
#define TISCI_DEV_MCSPi4_BUS_CLKSPiREF_CLK (0U)
#define TISCI_DEV_MCSPi4_BUS_VBUSP_CLK (1U)

```



```
#define TISCI_DEV_MCSPi3_BUS_IO_CLKSPiI_CLK (0U)
#define TISCI_DEV_MCSPi3_BUS_CLKSPiREF_CLK (1U)
#define TISCI_DEV_MCSPi3_BUS_VBUSP_CLK (2U)
#define TISCI_DEV_MCSPi3_BUS_IO_CLKSPiO_CLK (3U)
#define TISCI_DEV_MCU_MCSPi1_BUS_IO_CLKSPiI_CLK (0U)
#define TISCI_DEV_MCU_MCSPi1_BUS_CLKSPiREF_CLK (1U)
#define TISCI_DEV_MCU_MCSPi1_BUS_VBUSP_CLK (2U)
#define TISCI_DEV_MCU_MCSPi1_BUS_IO_CLKSPiO_CLK (3U)
#define TISCI_DEV_DEBUGSS_WRAP0_BUS_JTAG_TCK (0U)
#define TISCI_DEV_DEBUGSS_WRAP0_BUS_ATB_CLK (1U)
#define TISCI_DEV_DEBUGSS_WRAP0_BUS_TREXPT_CLK (2U)
#define TISCI_DEV_DEBUGSS_WRAP0_BUS_CORE_CLK (3U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK (0U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK_PARENT_ADPLLH_HSDIV_WRAP_M
(1U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK_PARENT_ADPLLJH_HSDIV_WRAP
(2U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK_PARENT_BOARD_0_BUS_MCU_CPT
(3U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK_PARENT_BOARD_0_BUS_CPT_S_RFT
(4U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK_PARENT_BOARD_0_BUS_MCU_EXT
(5U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK_PARENT_BOARD_0_BUS_EXT_REF
(6U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK_PARENT_WIZ8B2M4VSB_MAIN_0_BU
(7U)
#define TISCI_DEV_CBASS_INFRA0_BUS_GTC_CLOCK_1_CLK_PARENT_WIZ8B2M4VSB_MAIN_1_BU
(8U)
#define TISCI_DEV_CBASS_INFRA0_BUS_MAIN_SYSCLK0_2_CLK (9U)
#define TISCI_DEV_CBASS_INFRA0_BUS_MAIN_SYSCLK0_4_CLK (10U)
#define TISCI_DEV_STM0_BUS_CORE_CLK (0U)
#define TISCI_DEV_STM0_BUS_ATB_CLK (1U)
#define TISCI_DEV_STM0_BUS_VBUSP_CLK (2U)
#define TISCI_DEV_MCU_RT11_BUS_RT11_CLK (0U)
#define TISCI_DEV_MCU_RT11_BUS_RT11_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP
(1U)
#define TISCI_DEV_MCU_RT11_BUS_RT11_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(2U)
#define TISCI_DEV_MCU_RT11_BUS_RT11_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP
(3U)
```

```
#define TISCI_DEV_MCU_RTI1_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_
(4U)
#define TISCI_DEV_MCU_RTI1_BUS_VBUSB_CLK (5U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK (0U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_OSC0
(1U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(2U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_RCOS
(3U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_RCOS
(4U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK (5U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP0
(6U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP1
(7U)
#define TISCI_DEV_RTI0_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP2
(8U)
#define TISCI_DEV_RTI0_BUS_VBUSB_CLK (9U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK (0U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_OSC0
(1U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(2U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_RCOS
(3U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_RCOS
(4U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK (5U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP0
(6U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP1
(7U)
#define TISCI_DEV_RTI3_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP2
(8U)
#define TISCI_DEV_RTI3_BUS_VBUSB_CLK (9U)
#define TISCI_DEV_RTI1_BUS_RTI_CLK (0U)
#define TISCI_DEV_RTI1_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_OSC0
(1U)
#define TISCI_DEV_RTI1_BUS_RTI_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(2U)
```

```
#define TISCI_DEV_RTI1_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_RCOS
(3U)
#define TISCI_DEV_RTI1_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_RCOS
(4U)
#define TISCI_DEV_RTI1_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK (5U)
#define TISCI_DEV_RTI1_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP0
(6U)
#define TISCI_DEV_RTI1_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP1
(7U)
#define TISCI_DEV_RTI1_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP2
(8U)
#define TISCI_DEV_RTI1_BUS_VBUSEP_CLK (9U)
#define TISCI_DEV_MCU_RTI0_BUS_RTI_CLK (0U)
#define TISCI_DEV_MCU_RTI0_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_
(1U)
#define TISCI_DEV_MCU_RTI0_BUS_RTI_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(2U)
#define TISCI_DEV_MCU_RTI0_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_
(3U)
#define TISCI_DEV_MCU_RTI0_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_
(4U)
#define TISCI_DEV_MCU_RTI0_BUS_VBUSEP_CLK (5U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK (0U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_OSC0
(1U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(2U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_RCOS
(3U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_RCOS
(4U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK (5U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP0
(6U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP1
(7U)
#define TISCI_DEV_RTI2_BUS_RTI_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP2
(8U)
#define TISCI_DEV_RTI2_BUS_VBUSEP_CLK (9U)
#define TISCI_DEV_PSRAMECC0_BUS_CLK_CLK (0U)
#define TISCI_DEV_EFUSE0_BUS_VBUSEP_PLL_CLK_CLK (0U)
#define TISCI_DEV_EFUSE0_BUS_EFC1_CTL_FCLK (1U)
#define TISCI_DEV_EFUSE0_BUS_EFC0_CTL_FCLK (2U)
```

```

#define TISCI_DEV_MCASP0_BUS_AUX_CLK (0U)
#define TISCI_DEV_MCASP0_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK
(1U)
#define TISCI_DEV_MCASP0_BUS_AUX_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_C
(2U)
#define TISCI_DEV_MCASP0_BUS_AUX_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(3U)
#define TISCI_DEV_MCASP0_BUS_AUX_CLK_PARENT_ADPLLJLM_HSDIV_WRAP_MAIN_2_BUS_HSI
(4U)
#define TISCI_DEV_MCASP0_BUS_AUX_CLK_PARENT_CLOCKDIVIDER_MCASP_ARM1_PLL_DIV_BU
(5U)
#define TISCI_DEV_MCASP0_BUS_AUX_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(6U)
#define TISCI_DEV_MCASP0_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP0
(7U)
#define TISCI_DEV_MCASP0_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP1
(8U)
#define TISCI_DEV_MCASP0_BUS_VBUSP_CLK (9U)
#define TISCI_DEV_MCASP0_BUS_MCASP_AHCLKX_PIN (10U)
#define TISCI_DEV_MCASP0_BUS_MCASP_AHCLKR_PIN (11U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK (0U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK
(1U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_C
(2U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(3U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK_PARENT_ADPLLJLM_HSDIV_WRAP_MAIN_2_BUS_HSI
(4U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK_PARENT_CLOCKDIVIDER_MCASP_ARM1_PLL_DIV_BU
(5U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(6U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP0
(7U)
#define TISCI_DEV_MCASP1_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP1
(8U)
#define TISCI_DEV_MCASP1_BUS_VBUSP_CLK (9U)
#define TISCI_DEV_MCASP1_BUS_MCASP_AHCLKX_PIN (10U)
#define TISCI_DEV_MCASP1_BUS_MCASP_AHCLKR_PIN (11U)
#define TISCI_DEV_MCASP2_BUS_AUX_CLK (0U)
#define TISCI_DEV_MCASP2_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK
(1U)

```

```
#define TISCI_DEV_MCASP2_BUS_AUX_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_C
(2U)
#define TISCI_DEV_MCASP2_BUS_AUX_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(3U)
#define TISCI_DEV_MCASP2_BUS_AUX_CLK_PARENT_ADPLLJLM_HSDIV_WRAP_MAIN_2_BUS_HSI
(4U)
#define TISCI_DEV_MCASP2_BUS_AUX_CLK_PARENT_CLOCKDIVIDER_MCASP_ARM1_PLL_DIV_BU
(5U)
#define TISCI_DEV_MCASP2_BUS_AUX_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(6U)
#define TISCI_DEV_MCASP2_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP0
(7U)
#define TISCI_DEV_MCASP2_BUS_AUX_CLK_PARENT_BOARD_0_HFOSC1_CLK_DUP1
(8U)
#define TISCI_DEV_MCASP2_BUS_VBUSP_CLK (9U)
#define TISCI_DEV_MCASP2_BUS_MCASP_AHCLKX_PIN (10U)
#define TISCI_DEV_MCASP2_BUS_MCASP_AHCLKR_PIN (11U)
#define TISCI_DEV_MCU_ARMSS0_BUS_INTERFACE0_CLK (0U)
#define TISCI_DEV_MCU_ARMSS0_BUS_CPU0_CLK (1U)
#define TISCI_DEV_MCU_ARMSS0_BUS_CPU0_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP_0_BUS
(2U)
#define TISCI_DEV_MCU_ARMSS0_BUS_CPU0_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP_0_BUS
(3U)
#define TISCI_DEV_MCU_ARMSS0_BUS_INTERFACE1_CLK (4U)
#define TISCI_DEV_MCU_ARMSS0_BUS_INTERFACE0_PHASE (5U)
#define TISCI_DEV_MCU_ARMSS0_BUS_INTERFACE0_PHASE_PARENT_K3_PLL_CTRL_WRAP_WKU
(6U)
#define TISCI_DEV_MCU_ARMSS0_BUS_INTERFACE1_PHASE (7U)
#define TISCI_DEV_MCU_ARMSS0_BUS_INTERFACE1_PHASE_PARENT_K3_PLL_CTRL_WRAP_WKU
(8U)
#define TISCI_DEV_MCU_ARMSS0_BUS_CPU1_CLK (9U)
#define TISCI_DEV_MCU_ARMSS0_BUS_CPU1_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP_0_BUS
(10U)
#define TISCI_DEV_MCU_ARMSS0_BUS_CPU1_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP_0_BUS
(11U)
#define TISCI_DEV_CCDEBUGSS0_BUS_ATB1_CLK (0U)
#define TISCI_DEV_CCDEBUGSS0_BUS_ATB0_CLK (1U)
#define TISCI_DEV_CCDEBUGSS0_BUS_SYS_CLK (2U)
#define TISCI_DEV_CCDEBUGSS0_BUS_DBG_CLK (3U)
#define TISCI_DEV_CCDEBUGSS0_BUS_CFG_CLK (4U)
#define TISCI_DEV_WKUP_CTRL_MMR0_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_MCU_CBASS_FW0_BUS_MCU_SYSCLK0_4_CLK (0U)
```

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#define TISCI_DEV_MCU_CBASS_FW0_BUS_MCU_SYSCLK0_2_CLK (1U)
#define TISCI_DEV_MCU_CPSW0_BUS_GMII1_MR_CLK (0U)
#define TISCI_DEV_MCU_CPSW0_BUS_RGMII_MHZ_250_CLK (1U)
#define TISCI_DEV_MCU_CPSW0_BUS_CPTS_RFT_CLK (2U)
#define TISCI_DEV_MCU_CPSW0_BUS_GMII1_MT_CLK (3U)
#define TISCI_DEV_MCU_CPSW0_BUS_RGMII_MHZ_5_CLK (4U)
#define TISCI_DEV_MCU_CPSW0_BUS_RGMII_MHZ_50_CLK (5U)
#define TISCI_DEV_MCU_CPSW0_BUS_RMII_MHZ_50_CLK (6U)
#define TISCI_DEV_MCU_CPSW0_BUS_RMII_MHZ_50_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0 (7U)
#define TISCI_DEV_MCU_CPSW0_BUS_RMII_MHZ_50_CLK_PARENT_BOARD_0_BUS_MCU_RMII1_F (8U)
#define TISCI_DEV_MCU_CPSW0_BUS_GMII_RFT_CLK (9U)
#define TISCI_DEV_MCU_CPSW0_BUS_CPPI_CLK_CLK (10U)
#define TISCI_DEV_MCU_CPSW0_BUS_CPTS_GENF0_0 (11U)
#define TISCI_DEV_SERDES0_BUS_IP3_LN0_TXRCLK (0U)
#define TISCI_DEV_SERDES0_BUS_REFCLKPP (1U)
#define TISCI_DEV_SERDES0_BUS_CLK (2U)
#define TISCI_DEV_SERDES0_BUS_IP2_LN0_TXRCLK (3U)
#define TISCI_DEV_SERDES0_BUS_LI_REFCLK (4U)
#define TISCI_DEV_SERDES0_BUS_LI_REFCLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP (5U)
#define TISCI_DEV_SERDES0_BUS_LI_REFCLK_PARENT_BOARD_0_HFOSC1_CLK (6U)
#define TISCI_DEV_SERDES0_BUS_LI_REFCLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_C (7U)
#define TISCI_DEV_SERDES0_BUS_LI_REFCLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_F (8U)
#define TISCI_DEV_SERDES0_BUS_REFCLKPN (9U)
#define TISCI_DEV_SERDES0_BUS_LN0_TXCLK (10U)
#define TISCI_DEV_SERDES0_BUS_LN0_RXCLK (11U)
#define TISCI_DEV_SERDES1_BUS_IP3_LN0_TXRCLK (0U)
#define TISCI_DEV_SERDES1_BUS_REFCLKPP (1U)
#define TISCI_DEV_SERDES1_BUS_CLK (2U)
#define TISCI_DEV_SERDES1_BUS_IP1_LN0_TXRCLK (3U)
#define TISCI_DEV_SERDES1_BUS_IP2_LN0_TXRCLK (4U)
#define TISCI_DEV_SERDES1_BUS_RI_REFCLK (5U)
#define TISCI_DEV_SERDES1_BUS_RI_REFCLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP (6U)
#define TISCI_DEV_SERDES1_BUS_RI_REFCLK_PARENT_BOARD_0_HFOSC1_CLK (7U)

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#define TISCI_DEV_SERDES1_BUS_RI_REFCLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_C
(8U)
#define TISCI_DEV_SERDES1_BUS_RI_REFCLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_I
(9U)
#define TISCI_DEV_SERDES1_BUS_REFCLKPN (10U)
#define TISCI_DEV_SERDES1_BUS_LN0_TXCLK (11U)
#define TISCI_DEV_SERDES1_BUS_LN0_RXCLK (12U)
#define TISCI_DEV_OLDI_TX_CORE_MAIN_0_BUS_OLDI_PLL_CLK (0U)
#define TISCI_DEV_OLDI_TX_CORE_MAIN_0_BUS_OLDI_0_FWD_P_CLK_BUS_IN1_CLOCKDIVIDER
(1U)
#define TISCI_DEV_OLDI_TX_CORE_MAIN_0_BUS_OLDI_0_FWD_P_CLK_BUS_IN0_CLOCKDIVIDER
(2U)
#define TISCI_DEV_MCU_ADC1_BUS_VBUS_CLK (0U)
#define TISCI_DEV_MCU_ADC1_BUS_SYS_CLK (1U)
#define TISCI_DEV_MCU_ADC1_BUS_ADC_CLK (2U)
#define TISCI_DEV_MCU_ADC1_BUS_ADC_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKU
(3U)
#define TISCI_DEV_MCU_ADC1_BUS_ADC_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_HS
(4U)
#define TISCI_DEV_MCU_ADC1_BUS_ADC_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_HS
(5U)
#define TISCI_DEV_MCU_ADC1_BUS_ADC_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(6U)
#define TISCI_DEV_MCU_ADC0_BUS_VBUS_CLK (0U)
#define TISCI_DEV_MCU_ADC0_BUS_SYS_CLK (1U)
#define TISCI_DEV_MCU_ADC0_BUS_ADC_CLK (2U)
#define TISCI_DEV_MCU_ADC0_BUS_ADC_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKU
(3U)
#define TISCI_DEV_MCU_ADC0_BUS_ADC_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_HS
(4U)
#define TISCI_DEV_MCU_ADC0_BUS_ADC_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_HS
(5U)
#define TISCI_DEV_MCU_ADC0_BUS_ADC_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(6U)
#define TISCI_DEV_WKUP_DMSC0_BUS_FUNC_32K_RT_CLK (0U)
#define TISCI_DEV_WKUP_DMSC0_BUS_FUNC_MOSC_CLK (1U)
#define TISCI_DEV_WKUP_DMSC0_BUS_VBUS_CLK (2U)
#define TISCI_DEV_WKUP_DMSC0_BUS_FUNC_32K_RC_CLK (3U)
#define TISCI_DEV_WKUP_DMSC0_BUS_SEC_EFC_FCLK (4U)
#define TISCI_DEV_WKUP_DMSC0_BUS_DAP_CLK (5U)
#define TISCI_DEV_WKUP_DMSC0_BUS_EXT_CLK (6U)
#define TISCI_DEV_MCU_PLL_MMR0_BUS_VBUSP_CLK (0U)
```

```

#define TISCI_DEV_MCU_SEC_MMR0_BUS_VBUSB_CLK (0U)
#define TISCI_DEV_GIC0_BUS_VCLK_CLK (0U)
#define TISCI_DEV_MCU_DEBUGSS0_BUS_ATB1_CLK (0U)
#define TISCI_DEV_MCU_DEBUGSS0_BUS_ATB0_CLK (1U)
#define TISCI_DEV_MCU_DEBUGSS0_BUS_SYS_CLK (2U)
#define TISCI_DEV_MCU_DEBUGSS0_BUS_CFG_CLK (3U)
#define TISCI_DEV_MCU_DEBUGSS0_BUS_ATB2_CLK (4U)
#define TISCI_DEV_MCU_DEBUGSS0_BUS_DBG_CLK (5U)
#define TISCI_DEV_MCU_DEBUGSS0_BUS_ATB3_CLK (6U)
#define TISCI_DEV_EQEP0_BUS_VBUS_CLK (0U)
#define TISCI_DEV_EQEP2_BUS_VBUS_CLK (0U)
#define TISCI_DEV_EQEP1_BUS_VBUS_CLK (0U)
#define TISCI_DEV_WKUP_GPIO0_BUS_MMR_CLK (0U)
#define TISCI_DEV_WKUP_GPIO0_BUS_MMR_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP_0_BUS_
(1U)
#define TISCI_DEV_WKUP_GPIO0_BUS_MMR_CLK_PARENT_K3_PLL_CTRL_WRAP_WKUP_0_BUS_
(2U)
#define TISCI_DEV_WKUP_GPIO0_BUS_MMR_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_W
(3U)
#define TISCI_DEV_WKUP_GPIO0_BUS_MMR_CLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_W
(4U)
#define TISCI_DEV_GPIO0_BUS_MMR_CLK (0U)
#define TISCI_DEV_GPIO1_BUS_MMR_CLK (0U)
#define TISCI_DEV_COMPUTE_CLUSTER_MSMC0_BUS_TB_SOC_VBUSB_DMISC_CLK
(0U)
#define TISCI_DEV_COMPUTE_CLUSTER_MSMC0_BUS_TB_SOC_VBUSB_DBG_CLK
(1U)
#define TISCI_DEV_COMPUTE_CLUSTER_MSMC0_BUS_MSMC_CLK (2U)
#define TISCI_DEV_COMPUTE_CLUSTER_MSMC0_BUS_TB_SOC_VBUSB_CFG_CLK
(3U)
#define TISCI_DEV_COMPUTE_CLUSTER_MSMC0_BUS_TB_SOC_GIC_CLK (4U)
#define TISCI_DEV_COMPUTE_CLUSTER_CPAC0_BUS_ARM0_CLK (0U)
#define TISCI_DEV_COMPUTE_CLUSTER_CPAC1_BUS_ARM1_CLK (0U)
#define TISCI_DEV_COMPUTE_CLUSTER_A53_0_BUS_ARM0_CLK (0U)
#define TISCI_DEV_COMPUTE_CLUSTER_A53_1_BUS_ARM0_CLK (0U)
#define TISCI_DEV_COMPUTE_CLUSTER_A53_2_BUS_ARM1_CLK (0U)
#define TISCI_DEV_COMPUTE_CLUSTER_A53_3_BUS_ARM1_CLK (0U)
#define TISCI_DEV_WKUP_CBASS0_BUS_WKUP_MCU_PLL_OUT_2_CLK (0U)
#define TISCI_DEV_WKUP_CBASS0_BUS_WKUP_MCU_PLL_OUT_4_CLK (1U)
#define TISCI_DEV_MCU_ROM0_BUS_CLK_CLK (0U)

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```
#define TISCI_DEV_K3_ARM_ATB_FUNNEL_3_32_MCU_0_BUS_DBG_CLK (0U)
#define TISCI_DEV_ESM0_BUS_CLK (0U)
#define TISCI_DEV_PRU_ICSSG2_BUS_RGMII_MHZ_5_CLK (0U)
#define TISCI_DEV_PRU_ICSSG2_BUS_WIZ1_TX_SLV_CLK (1U)
#define TISCI_DEV_PRU_ICSSG2_BUS_WIZ0_RX_SLV_CLK (2U)
#define TISCI_DEV_PRU_ICSSG2_BUS_VCLK_CLK (3U)
#define TISCI_DEV_PRU_ICSSG2_BUS_UCLK_CLK (4U)
#define TISCI_DEV_PRU_ICSSG2_BUS_WIZ0_TX_SLV_CLK (5U)
#define TISCI_DEV_PRU_ICSSG2_BUS_WIZ1_RX_SLV_CLK (6U)
#define TISCI_DEV_PRU_ICSSG2_BUS_PR1_RGMII1_RXC_I (7U)
#define TISCI_DEV_PRU_ICSSG2_BUS_RGMII_MHZ_250_CLK (8U)
#define TISCI_DEV_PRU_ICSSG2_BUS_RGMII_MHZ_50_CLK (9U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK (10U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_HS
(11U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS
(12U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK_PARENT_BOARD_0_BUS_MCU_CPTS_RFT_CLK
(13U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(14U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(15U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(16U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK_PARENT_WIZ8B2M4VSB_MAIN_0_BUS_LN0_TXCLK
(17U)
#define TISCI_DEV_PRU_ICSSG2_BUS_IEP_CLK_PARENT_WIZ8B2M4VSB_MAIN_1_BUS_LN0_TXCLK
(18U)
#define TISCI_DEV_PRU_ICSSG2_BUS_CORE_CLK (19U)
#define TISCI_DEV_PRU_ICSSG2_BUS_CORE_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_2_BU
(20U)
#define TISCI_DEV_PRU_ICSSG2_BUS_CORE_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_
(21U)
#define TISCI_DEV_PRU_ICSSG2_BUS_PR1_RGMII0_RXC_I (22U)
#define TISCI_DEV_PRU_ICSSG2_BUS_PR1_RGMII1_TXC_I (23U)
#define TISCI_DEV_PRU_ICSSG2_BUS_PR1_RGMII0_TXC_I (24U)
#define TISCI_DEV_PRU_ICSSG0_BUS_RGMII_MHZ_5_CLK (0U)
#define TISCI_DEV_PRU_ICSSG0_BUS_WIZ1_TX_SLV_CLK (1U)
#define TISCI_DEV_PRU_ICSSG0_BUS_WIZ0_RX_SLV_CLK (2U)
#define TISCI_DEV_PRU_ICSSG0_BUS_VCLK_CLK (3U)
```

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#define TISCI_DEV_PRU_ICSSG0_BUS_UCLK_CLK (4U)
#define TISCI_DEV_PRU_ICSSG0_BUS_WIZ0_TX_SLV_CLK (5U)
#define TISCI_DEV_PRU_ICSSG0_BUS_WIZ1_RX_SLV_CLK (6U)
#define TISCI_DEV_PRU_ICSSG0_BUS_PR1_RGMII1_RXC_I (7U)
#define TISCI_DEV_PRU_ICSSG0_BUS_RGMII_MHZ_250_CLK (8U)
#define TISCI_DEV_PRU_ICSSG0_BUS_RGMII_MHZ_50_CLK (9U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK (10U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK_PARENT_ADPLLH_HSDIV_WRAP_MCU_1_BUS_HS
(11U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK_PARENT_ADPLLHJM_HSDIV_WRAP_MAIN_0_BUS
(12U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK_PARENT_BOARD_0_BUS_MCU_CPTS_RFT_CLK
(13U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(14U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(15U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(16U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK_PARENT_WIZ8B2M4VSB_MAIN_0_BUS_LN0_TXCLK
(17U)
#define TISCI_DEV_PRU_ICSSG0_BUS_IEP_CLK_PARENT_WIZ8B2M4VSB_MAIN_1_BUS_LN0_TXCLK
(18U)
#define TISCI_DEV_PRU_ICSSG0_BUS_CORE_CLK (19U)
#define TISCI_DEV_PRU_ICSSG0_BUS_CORE_CLK_PARENT_ADPLLHJM_HSDIV_WRAP_MAIN_2_BU
(20U)
#define TISCI_DEV_PRU_ICSSG0_BUS_CORE_CLK_PARENT_ADPLLH_HSDIV_WRAP_MCU_1_BUS_
(21U)
#define TISCI_DEV_PRU_ICSSG0_BUS_PR1_RGMII0_RXC_I (22U)
#define TISCI_DEV_PRU_ICSSG0_BUS_PR1_RGMII1_TXC_I (23U)
#define TISCI_DEV_PRU_ICSSG0_BUS_PR1_RGMII0_TXC_I (24U)
#define TISCI_DEV_PRU_ICSSG0_BUS_WIZ1_TX_MST_CLK (25U)
#define TISCI_DEV_PRU_ICSSG0_BUS_WIZ0_TX_MST_CLK (26U)
#define TISCI_DEV_PRU_ICSSG1_BUS_RGMII_MHZ_5_CLK (0U)
#define TISCI_DEV_PRU_ICSSG1_BUS_WIZ1_TX_SLV_CLK (1U)
#define TISCI_DEV_PRU_ICSSG1_BUS_WIZ0_RX_SLV_CLK (2U)
#define TISCI_DEV_PRU_ICSSG1_BUS_VCLK_CLK (3U)
#define TISCI_DEV_PRU_ICSSG1_BUS_UCLK_CLK (4U)
#define TISCI_DEV_PRU_ICSSG1_BUS_WIZ0_TX_SLV_CLK (5U)
#define TISCI_DEV_PRU_ICSSG1_BUS_WIZ1_RX_SLV_CLK (6U)
#define TISCI_DEV_PRU_ICSSG1_BUS_PR1_RGMII1_RXC_I (7U)

```

```
#define TISCI_DEV_PRU_ICSSG1_BUS_RGMII_MHZ_250_CLK (8U)
#define TISCI_DEV_PRU_ICSSG1_BUS_RGMII_MHZ_50_CLK (9U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK (10U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_HS
(11U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS
(12U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK_PARENT_BOARD_0_BUS_MCU_CPTS_RFT_CLK
(13U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(14U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(15U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(16U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK_PARENT_WIZ8B2M4VSB_MAIN_0_BUS_LN0_TXCLK
(17U)
#define TISCI_DEV_PRU_ICSSG1_BUS_IEP_CLK_PARENT_WIZ8B2M4VSB_MAIN_1_BUS_LN0_TXCLK
(18U)
#define TISCI_DEV_PRU_ICSSG1_BUS_CORE_CLK (19U)
#define TISCI_DEV_PRU_ICSSG1_BUS_CORE_CLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_2_BU
(20U)
#define TISCI_DEV_PRU_ICSSG1_BUS_CORE_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_
(21U)
#define TISCI_DEV_PRU_ICSSG1_BUS_PR1_RGMII0_RXC_I (22U)
#define TISCI_DEV_PRU_ICSSG1_BUS_PR1_RGMII1_TXC_I (23U)
#define TISCI_DEV_PRU_ICSSG1_BUS_PR1_RGMII0_TXC_I (24U)
#define TISCI_DEV_MCU_ESM0_BUS_CLK (0U)
#define TISCI_DEV_ECAP0_BUS_VBUS_CLK (0U)
#define TISCI_DEV_WKUP_ESM0_BUS_CLK (0U)
#define TISCI_DEV_MCU_EFUSE0_BUS_VBUSP_CLK_CLK (0U)
#define TISCI_DEV_MCU_EFUSE0_BUS_EFC3_CTL_FCLK (1U)
#define TISCI_DEV_MCU_EFUSE0_BUS_EFC0_CTL_FCLK (2U)
#define TISCI_DEV_MCU_EFUSE0_BUS_EFC1_CTL_FCLK (3U)
#define TISCI_DEV_MCU_EFUSE0_BUS_EFC2_CTL_FCLK (4U)
#define TISCI_DEV_MCU_CTRL_MMR0_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_PSC0_BUS_CLK (0U)
#define TISCI_DEV_PSC0_BUS_SLOW_CLK (1U)
#define TISCI_DEV_CTRL_MMR0_BUS_VBUSP_CLK (0U)
#define TISCI_DEV_MCU_MCAN0_BUS_MCANSS_CCLK_CLK (0U)
```

```

#define TISCI_DEV_MCU_MCAN0_BUS_MCANSS_CCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(1U)
#define TISCI_DEV_MCU_MCAN0_BUS_MCANSS_CCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(2U)
#define TISCI_DEV_MCU_MCAN0_BUS_MCANSS_CCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(3U)
#define TISCI_DEV_MCU_MCAN0_BUS_MCANSS_CCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_
(4U)
#define TISCI_DEV_MCU_MCAN0_BUS_MCANSS_HCLK_CLK (5U)
#define TISCI_DEV_MCU_MCAN1_BUS_MCANSS_CCLK_CLK (0U)
#define TISCI_DEV_MCU_MCAN1_BUS_MCANSS_CCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(1U)
#define TISCI_DEV_MCU_MCAN1_BUS_MCANSS_CCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(2U)
#define TISCI_DEV_MCU_MCAN1_BUS_MCANSS_CCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU
(3U)
#define TISCI_DEV_MCU_MCAN1_BUS_MCANSS_CCLK_CLK_PARENT_MX_WAKEUP_GS80_WKUP_
(4U)
#define TISCI_DEV_MCU_MCAN1_BUS_MCANSS_HCLK_CLK (5U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_VBUS_CLK (0U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_BYP_4X_CLK (1U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_CTL_CLK_BUS_IN1_ADPLLLJM_WRAP_MAIN_3_BUS_CLI
(2U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_TCLK (3U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_PHY_CTL_CLK_BUS_IN1_ADPLLLJM_WRAP_MAIN_3_BU
(4U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_PHY_CTL_CLK_BUS_IN0_ADPLLLJM_WRAP_MAIN_3_BU
(5U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_CFG_CLK (6U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_CTL_CLK_BUS_IN0_ADPLLLJM_WRAP_MAIN_3_BUS_CLI
(7U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_BYP_CLK_BUS_IN1_ADPLLLJM_WRAP_MAIN_3_BUS_CLI
(8U)
#define TISCI_DEV_DDRSS0_BUS_DDRSS_BYP_CLK_BUS_IN0_ADPLLLJM_WRAP_MAIN_3_BUS_CLI
(9U)
#define TISCI_DEV_MCU_NAVSS0_BUS_UDMASS_VD2CLK (0U)
#define TISCI_DEV_MCU_NAVSS0_BUS_CPSW0CLK (1U)
#define TISCI_DEV_MCU_NAVSS0_BUS_MODSS_VD2CLK (2U)
#define TISCI_DEV_MCU_NAVSS0_BUS_PDMA_MCU1CLK (3U)
#define TISCI_DEV_MCU_FSS0_BUS_HPB_CLKX1_INV_CLK (0U)
#define TISCI_DEV_MCU_FSS0_BUS_VBUS_CLK (1U)
#define TISCI_DEV_MCU_FSS0_BUS_OSPI1_ICLK_CLK (2U)

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```
#define TISCI_DEV_MCU_FSS0_BUS_OSPI1_ICLK_CLK_PARENT_BOARD_0_BUS_MCU_OSPI1DQS  
(3U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI1_ICLK_CLK_PARENT_FSS_MCU_0_BUS_OSPI1_OCLK_CLK  
(4U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI0_RCLK_CLK (5U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI0_RCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_F  
(6U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI0_RCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_F  
(7U)  
#define TISCI_DEV_MCU_FSS0_BUS_HPB_CLKX2_CLK (8U)  
#define TISCI_DEV_MCU_FSS0_BUS_HPB_CLKX2_INV_CLK (9U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI0_ICLK_CLK (10U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI0_ICLK_CLK_PARENT_BOARD_0_BUS_MCU_OSPI0DQS  
(11U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI0_ICLK_CLK_PARENT_FSS_MCU_0_BUS_OSPI0_OCLK_CLK  
(12U)  
#define TISCI_DEV_MCU_FSS0_BUS_HPB_CLKX1_CLK (13U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI0_DQS_CLK (14U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI1_DQS_CLK (15U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI1_RCLK_CLK (16U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI1_RCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_F  
(17U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI1_RCLK_CLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_F  
(18U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI0_OCLK_CLK (19U)  
#define TISCI_DEV_MCU_FSS0_BUS_OSPI1_OCLK_CLK (20U)  
#define TISCI_DEV_DFTSS0_BUS_VBUSEP_CLK_CLK (0U)  
#define TISCI_DEV_WKUP_GPIOMUX_INTRTR0_BUS_INTR_CLK (0U)  
#define TISCI_DEV_GPIOMUX_INTRTR0_BUS_INTR_CLK (0U)  
#define TISCI_DEV_MAIN2MCU_LVL_INTRTR0_BUS_INTR_CLK (0U)  
#define TISCI_DEV_MAIN2MCU_PLS_INTRTR0_BUS_INTR_CLK (0U)  
#define TISCI_DEV_GPU0_BUS_MEM_CLK (0U)  
#define TISCI_DEV_GPU0_BUS_HYD_CORE_CLK (1U)  
#define TISCI_DEV_GPU0_BUS_SGX_CORE_CLK (2U)  
#define TISCI_DEV_GPU0_BUS_SYS_CLK (3U)  
#define TISCI_DEV_PDMA_DEBUG0_BUS_VCLK (0U)  
#define TISCI_DEV_PDMA0_BUS_VCLK (0U)  
#define TISCI_DEV_PDMA1_BUS_VCLK (0U)  
#define TISCI_DEV_MCU_PDMA0_BUS_VCLK (0U)  
#define TISCI_DEV_MCU_PDMA1_BUS_VCLK (0U)  
#define TISCI_DEV_MCU_MSRAM0_BUS_CCLK_CLK (0U)
```

```

#define TISCI_DEV_MCU_MSRAM0_BUS_VCLK_CLK (1U)
#define TISCI_DEV_CMPEVENT_INTRTR0_BUS_INTR_CLK (0U)
#define TISCI_DEV_DEBUGSUSPENDRTR0_BUS_INTR_CLK (0U)
#define TISCI_DEV_TIMESYNC_INTRTR0_BUS_INTR_CLK (0U)
#define TISCI_DEV_CBASS_DEBUG0_BUS_MAIN_SYSCLK0_2_CLK (0U)
#define TISCI_DEV_CBASS_DEBUG0_BUS_MAIN_SYSCLK0_4_CLK (1U)
#define TISCI_DEV_CBASS_FW0_BUS_MAIN_SYSCLK0_2_CLK (0U)
#define TISCI_DEV_CBASS_FW0_BUS_MAIN_SYSCLK0_4_CLK (1U)
#define TISCI_DEV_MCU_CBASS_DEBUG0_BUS_MCU_SYSCLK0_2_CLK (0U)
#define TISCI_DEV_WKUP_CBASS_FW0_BUS_WKUP_MCU_PLL_OUT_2_CLK (0U)
#define TISCI_DEV_PCIE0_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN5_BOARD_0_BUS_EXT_REFCLK1 (0U)
#define TISCI_DEV_PCIE0_BUS_PCIE_CBA_CLK (1U)
#define TISCI_DEV_PCIE0_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN3_BOARD_0_BUS_CPTS_RFT_CLK (2U)
#define TISCI_DEV_PCIE0_BUS_PCIE_TXI0_CLK (3U)
#define TISCI_DEV_PCIE0_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN1_ADPLLJLM_HSDIV_WRAP_MAIN (4U)
#define TISCI_DEV_PCIE0_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN0_ADPLLM_HSDIV_WRAP_MCU_1 (5U)
#define TISCI_DEV_PCIE0_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN4_BOARD_0_BUS_MCU_EXT_REFCLK1 (6U)
#define TISCI_DEV_PCIE0_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN2_BOARD_0_BUS_MCU_CPTS_RFT_CLK (7U)
#define TISCI_DEV_PCIE0_BUS_PCIE_TXR1_CLK (8U)
#define TISCI_DEV_PCIE0_BUS_PCIE_TXR0_CLK (9U)
#define TISCI_DEV_PCIE1_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN5_BOARD_0_BUS_EXT_REFCLK1 (0U)
#define TISCI_DEV_PCIE1_BUS_PCIE_CBA_CLK (1U)
#define TISCI_DEV_PCIE1_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN3_BOARD_0_BUS_CPTS_RFT_CLK (2U)
#define TISCI_DEV_PCIE1_BUS_PCIE_TXI0_CLK (3U)
#define TISCI_DEV_PCIE1_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN1_ADPLLJLM_HSDIV_WRAP_MAIN (4U)
#define TISCI_DEV_PCIE1_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN0_ADPLLM_HSDIV_WRAP_MCU_1 (5U)
#define TISCI_DEV_PCIE1_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN4_BOARD_0_BUS_MCU_EXT_REFCLK1 (6U)
#define TISCI_DEV_PCIE1_BUS_PCIE_CPTS_RCLK_CLK_BUS_IN2_BOARD_0_BUS_MCU_CPTS_RFT_CLK (7U)
#define TISCI_DEV_PCIE1_BUS_PCIE_TXR0_CLK (8U)

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```
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK (0U)
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK_PARENT_ADPLLH_HSDIV_WRAP_MCU_1_BUS_HSDIV
(1U)
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK_PARENT_ADPLLJM_HSDIV_WRAP_MAIN_0_BUS_HSDIV
(2U)
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK_PARENT_BOARD_0_BUS_MCU_CPTS_RFT_CLK
(3U)
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK_PARENT_BOARD_0_BUS_CPTS_RFT_CLK
(4U)
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK_PARENT_BOARD_0_BUS_MCU_EXT_REFCLK0
(5U)
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK_PARENT_BOARD_0_BUS_EXT_REFCLK1
(6U)
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK_PARENT_WIZ8B2M4VSB_MAIN_0_BUS_LN0_TXCLK
(7U)
#define TISCI_DEV_GTC0_BUS_VBUSEP_CLK_PARENT_WIZ8B2M4VSB_MAIN_1_BUS_LN0_TXCLK
(8U)
#define TISCI_DEV_WKUP_VTM0_BUS_FIX_REF_CLK (0U)
#define TISCI_DEV_WKUP_VTM0_BUS_VBUSEP_CLK (1U)
#define TISCI_DEV_MMCSO0_BUS_EMMCSDSS_VBUS_CLK (0U)
#define TISCI_DEV_MMCSO0_BUS_EMMCSDSS_XIN_CLK (1U)
#define TISCI_DEV_MCU_ECC_AGGR0_BUS_AGGR_CLK (0U)
#define TISCI_DEV_ECC_AGGR1_BUS_AGGR_CLK (0U)
#define TISCI_DEV_ECC_AGGR2_BUS_AGGR_CLK (0U)
#define TISCI_DEV_MCU_ECC_AGGR1_BUS_AGGR_CLK (0U)
#define TISCI_DEV_WKUP_ECC_AGGR0_BUS_AGGR_CLK (0U)
#define TISCI_DEV_ECC_AGGR0_BUS_AGGR_CLK (0U)
#define TISCI_DEV_MCU_PSRAM0_BUS_CLK_CLK (0U)
#define TISCI_DEV_GS80PRG_SOC_WRAP_WKUP_0_BUS_OSC_CLK (0U)
#define TISCI_DEV_GS80PRG_SOC_WRAP_WKUP_0_BUS_CLK (1U)
#define TISCI_DEV_GS80PRG_MCU_WRAP_WKUP_0_BUS_OSC_CLK (0U)
#define TISCI_DEV_GS80PRG_MCU_WRAP_WKUP_0_BUS_CLK (1U)
#define TISCI_DEV_MCU_CBASS0_BUS_MCU_SYSCLK0_8_CLK (0U)
#define TISCI_DEV_MCU_CBASS0_BUS_MCU_SYSCLK0_4_CLK (1U)
#define TISCI_DEV_MCU_CBASS0_BUS_MCU_SYSCLK0_2_CLK (2U)
#define TISCI_DEV_MX_EFUSE_MAIN_CHAIN_MAIN_0_BUS_UNDEFINEDCHAIN1_FCLK
(0U)
#define TISCI_DEV_MX_EFUSE_MAIN_CHAIN_MAIN_0_BUS_UNDEFINEDCHAIN0_FCLK
(1U)
#define TISCI_DEV_MX_EFUSE_MCU_CHAIN_MCU_0_BUS_UNDEFINEDCHAIN1_FCLK
(0U)
```

```

#define TISCI_DEV_MX_EFUSE_MCU_CHAIN_MCU_0_BUS_UNDEFINEDCHAIN0_FCLK
(1U)
#define TISCI_DEV_MX_EFUSE_MCU_CHAIN_MCU_0_BUS_UNDEFINEDCHAIN2_FCLK
(2U)
#define TISCI_DEV_BOARD0_BUS_SCL3 (0U)
#define TISCI_DEV_BOARD0_BUS_SCL2 (1U)
#define TISCI_DEV_BOARD0_BUS_SCL1 (2U)
#define TISCI_DEV_BOARD0_BUS_SCL0 (3U)
#define TISCI_DEV_BOARD0_BUS_PRG2_RGMII2_TCLK (4U)
#define TISCI_DEV_BOARD0_BUS_MCU_OSPI1CLK (5U)
#define TISCI_DEV_BOARD0_BUS_PRG1_RGMII1_TCLK (6U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1P (7U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1P_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_
(8U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1P_PARENT_BOARD_0_HFOSC1_CLK
(9U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1P_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_CL
(10U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1P_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_HS
(11U)
#define TISCI_DEV_BOARD0_BUS_MCU_OSPI1LBCLKO (12U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK (13U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKU
(14U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKU
(15U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_C
(16U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_C
(17U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_H
(18U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_H
(19U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_H
(20U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_0_BUS_H
(21U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_C
(22U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKU
(23U)

```



```
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_H
(24U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_H
(25U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_H
(26U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_H
(27U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKU
(28U)
#define TISCI_DEV_BOARD0_BUS_MCU_OBSCLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(29U)
#define TISCI_DEV_BOARD0_BUS_PRG2_RGMII1_TCLK (30U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1M (31U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1M_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_
(32U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1M_PARENT_BOARD_0_HFOSC1_CLK
(33U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1M_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_CH
(34U)
#define TISCI_DEV_BOARD0_BUS_REFCLK1M_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_HS
(35U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK (36U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_BOARD_0_HFOSC1_CLK
(37U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_OS
(38U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_CLKO
(39U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLLJM_WRAP_MAIN_1_BUS_CLKOUT_CH
(40U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_GLUELOGIC_LFOSC_CLK_BUS_OUT
(41U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_2_BUS_CLKO
(42U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLLJM_WRAP_MAIN_4_BUS_CLKOUT_CH
(43U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLM_WRAP_MAIN_6_BUS_CLKOUT_CLK
(44U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLLJM_WRAP_MAIN_3_BUS_CLKOUT_CH
(45U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_CLKOU
(46U)
```

```

#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_HSDI
(47U)
#define TISCI_DEV_BOARD0_BUS_OBSCLK_PARENT_ADPLLM_WRAP_MAIN_7_BUS_CLKOUT_CLK
(48U)
#define TISCI_DEV_BOARD0_BUS_PRG0_RGMII1_TCLK (49U)
#define TISCI_DEV_BOARD0_BUS_MCU_OSPI0CLK (50U)
#define TISCI_DEV_BOARD0_BUS_DSS0PCLK (51U)
#define TISCI_DEV_BOARD0_BUS_PRG0_RGMII2_TCLK (52U)
#define TISCI_DEV_BOARD0_BUS_WKUP_SCL0 (53U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0P (54U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0P_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_
(55U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0P_PARENT_BOARD_0_HFOSC1_CLK
(56U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0P_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_CL
(57U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0P_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_HS
(58U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0M (59U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0M_PARENT_MX_WAKEUP_GS80_WKUP_0_BUS_WKUP_
(60U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0M_PARENT_BOARD_0_HFOSC1_CLK
(61U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0M_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_CL
(62U)
#define TISCI_DEV_BOARD0_BUS_REFCLK0M_PARENT_ADPLLLJM_HSDIV_WRAP_MAIN_0_BUS_HS
(63U)
#define TISCI_DEV_BOARD0_BUS_MCU_OSPI0LBCLKO (64U)
#define TISCI_DEV_BOARD0_BUS_MCU_CLKOUT (65U)
#define TISCI_DEV_BOARD0_BUS_MCU_CLKOUT_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_C
(66U)
#define TISCI_DEV_BOARD0_BUS_MCU_CLKOUT_PARENT_ADPLLM_HSDIV_WRAP_MCU_1_BUS_C
(67U)
#define TISCI_DEV_BOARD0_BUS_MCU_SCL0 (68U)
#define TISCI_DEV_BOARD0_BUS_SYSCLKOUT (69U)
#define TISCI_DEV_BOARD0_BUS_MCU_SYSCLKOUT (70U)
#define TISCI_DEV_BOARD0_BUS_PRG1_RGMII1_RCLK (71U)
#define TISCI_DEV_BOARD0_BUS_PRG1_RGMII2_RCLK (72U)
#define TISCI_DEV_BOARD0_BUS_GPMCCLK (73U)
#define TISCI_DEV_BOARD0_BUS_MCASP2AHCLKX (74U)
#define TISCI_DEV_BOARD0_BUS_MCASP2AHCLKR (75U)
#define TISCI_DEV_BOARD0_BUS_PRG2_RGMII2_RCLK (76U)

```

```
#define TISCI_DEV_BOARD0_BUS_CPTS_RFT_CLK (77U)
#define TISCI_DEV_BOARD0_BUS_MCASP0ACLKR (78U)
#define TISCI_DEV_BOARD0_BUS_MCASP0ACLKX (79U)
#define TISCI_DEV_BOARD0_BUS_EXT_REFCLK1 (80U)
#define TISCI_DEV_BOARD0_BUS_PRG0_RGMII2_RCLK (81U)
#define TISCI_DEV_BOARD0_BUS_MCU_OSPI0DQS (82U)
#define TISCI_DEV_BOARD0_BUS_USB0REFCLKP (83U)
#define TISCI_DEV_BOARD0_BUS_DSS0EXTCLKIN (84U)
#define TISCI_DEV_BOARD0_BUS_SPI1CLK (85U)
#define TISCI_DEV_BOARD0_BUS_MCASP2ACLKR (86U)
#define TISCI_DEV_BOARD0_BUS_MCASP1ACLKX (87U)
#define TISCI_DEV_BOARD0_BUS_MCASP1ACLKR (88U)
#define TISCI_DEV_BOARD0_BUS_MCASP2ACLKX (89U)
#define TISCI_DEV_BOARD0_BUS_MCU_RMII1_REFCLK (90U)
#define TISCI_DEV_BOARD0_BUS_MCU_CPTS_RFT_CLK (91U)
#define TISCI_DEV_BOARD0_BUS_MCU_RGMII1_TCLK (92U)
#define TISCI_DEV_BOARD0_BUS_MCU_SPI0CLK (93U)
#define TISCI_DEV_BOARD0_BUS_MCU_SPI1CLK (94U)
#define TISCI_DEV_BOARD0_BUS_PRG0_RGMII1_RCLK (95U)
#define TISCI_DEV_BOARD0_BUS_SPI2CLK (96U)
#define TISCI_DEV_BOARD0_BUS_WKUP_TCK (97U)
#define TISCI_DEV_BOARD0_BUS_SPI3CLK (98U)
#define TISCI_DEV_BOARD0_BUS_USB0REFCLKM (99U)
#define TISCI_DEV_BOARD0_BUS_MCU_RGMII1_RCLK (100U)
#define TISCI_DEV_BOARD0_BUS_MCASP0AHCLKR (101U)
#define TISCI_DEV_BOARD0_BUS_MCU_EXT_REFCLK0 (102U)
#define TISCI_DEV_BOARD0_BUS_MCASP0AHCLKX (103U)
#define TISCI_DEV_BOARD0_BUS_CCDC0_PCLK (104U)
#define TISCI_DEV_BOARD0_HFOSC1_CLK (105U)
#define TISCI_DEV_BOARD0_BUS_MCU_OSPI1DQS (106U)
#define TISCI_DEV_BOARD0_BUS_MCASP1AHCLKX (107U)
#define TISCI_DEV_BOARD0_BUS_PCIE1REFCLKM (108U)
#define TISCI_DEV_BOARD0_BUS_MCASP1AHCLKR (109U)
#define TISCI_DEV_BOARD0_BUS_PCIE1REFCLKP (110U)
#define TISCI_DEV_BOARD0_BUS_PRG2_RGMII1_RCLK (111U)
#define TISCI_DEV_BOARD0_BUS_SPI0CLK (112U)
```

4.1.26 TISCI_ISC_CC_ID

Special ISC ID to refer to compute cluster privid registers

Definition

```
#define TISCI_ISC_CC_ID (160U)
```

Comments None

Constraints None

See Also None

4.2 Typedefs and Data Structures

4.2.1 Sciclient_ConfigPrms_t

Initialization parameters for sciclient. Pointer to this is passed to #Sciclient_init.

Definition

```
typedef struct {  
    uint32_t opModeFlag; Sciclient_BoardCfgPrms_t * pBoardCfgPrms;  
} Sciclient_ConfigPrms_t;
```

Fields

- opModeFlag : Operation mode for the Sciclient Service API. Refer to ref Sciclient_ServiceOperationMode for valid values.
- pBoardCfgPrms : NULL will result in using default board configuration.
Refer #Sciclient_BoardCfgPrms_t

Comments None

Constraints None

See Also None

4.2.2 Sciclient_ReqPrm_t

Input parameters for #Sciclient_service function.

Definition

```
typedef struct {  
    uint16_t messageType; uint32_t flags; const uint8_t * pReqPayload; uint32_t reqPayloadSize;  
    uint32_t timeout;  
} Sciclient_ReqPrm_t;
```

Fields

- messageType : [IN] Type of message.
- flags : [IN] Flags for messages that are being transmitted.
(Refer ref Tisci_ReqFlags)
- pReqPayload : [IN] Pointer to the payload to be transmitted

- reqPayloadSize : [IN] Size of the payload to be transmitted (in bytes)
- timeout : [IN] Timeout in ms for receiving response
(Refer ref Sciclient_ServiceOperationTimeout)

Comments None

Constraints None

See Also None

4.2.3 Sciclient_RespPrm_t

Output parameters for #Sciclient_service function.

Definition

```
typedef struct {
    uint32_t flags; uint8_t * pRespPayload; uint32_t respPayloadSize;
} Sciclient_RespPrm_t;
```

Fields

- flags : [OUT] Flags of message: Refer ref Tisci_RespFlags.
- pRespPayload : [IN] Pointer to the received payload. The pointer is an input. The API will populate this with the firmware response upto the size mentioned in respPayloadSize. Please ensure respPayloadSize bytes are allocated.
- respPayloadSize : [IN] Size of the response payload (in bytes)

Comments None

Constraints None

See Also None

4.3 API Definition

4.3.1 Sciclient_loadFirmware

Loads the DMSC firmware. This is typically called by SBL. Load firmware does not require calling the #Sciclient_init function.

Requirement: DOX_REQ_TAG (PDK-2137) , DOX_REQ_TAG (PDK-2138)

Syntax

```
int32_t Sciclient_loadFirmware(const uint32_t *pSciclient_firmware);
```

Arguments

pSciclient_firmware : [IN] Pointer to signed SYSFW binary

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.2 Sciclient_init

This API is called once for registering interrupts and creating semaphore handles to be able to talk to the firmware. The application should assume that the firmware is pre-loaded while calling the #Sciclient_init API. The firmware should have been loaded either via GEL or via the SBL prior to the application calling the #Sciclient_init. If a void pointer is passed, default values will be used, else the values passed will be used.

Requirement: DOX_REQ_TAG (PDK-2146)

Syntax

```
int32_t Sciclient_init(const Sciclient_ConfigPrms_t * pCfgPrms);
```

Arguments

pCfgPrms : [IN] Pointer to #Sciclient_ConfigPrms_t

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.3 Sciclient_service

This API allows communicating with the System firmware which can be called to perform various functions in the system. Core sciclient function for transmitting payload and receiving the response. The caller is expected to allocate memory for the input request parameter (Refer #Sciclient_ReqPrm_t). This involves setting the message type being communicated to the firmware, the response flags, populate the payload of the message based on the inputs in the files sciclient_fmwmessages.h, sciclient_fmwrmmessages.h, sciclient_fmwwsecmessages.h and sciclient_fmwwcommonmessages.h. Since the payload is considered a stream of bytes in this API, the caller should also populate the size of this stream in reqPayloadSize. The timeout is used to determine for what amount of iterations the API would wait for their operation to complete.

To make sure the response is captured correctly the caller should also allocate the space for #Sciclient_RespPrm_t parameters. The caller should populate the pointer to the pRespPayload and the size respPayloadSize. The API would populate the response flags to indicate any firmware specific errors and also populate the memory pointed by pRespPayload till the size given in respPayloadSize.

Requirement: DOX_REQ_TAG (PDK-2142) , DOX_REQ_TAG (PDK-2141) , DOX_REQ_TAG (PDK-2140) , DOX_REQ_TAG (PDK-2139)

Syntax

```
int32_t Sciclient_service(const Sciclient_ReqPrm_t * pReqPrm, Sciclient_RespPrm_t * pRespPrm);
```

Arguments

pReqPrm : [IN] Pointer to #Sciclient_ReqPrm_t

pRespPrm : [OUT] Pointer to #Sciclient_RespPrm_t

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.4 Sciclient_deinit

De-initialization of sciclient. This de-initialization is specific to the application. It only de-initializes the semaphores, interrupts etc. which are initialized in #Sciclient_init. It does not de-initialize the system firmware.

Requirement: DOX_REQ_TAG (PDK-2146)

Syntax

```
int32_t Sciclient_deinit( void);
```

Arguments

void :

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.5 Sciclient_pmSetModuleState

Message to set the hardware block/module state This is used to request or release a device. For example: When the device is requested for operation, state is set to MSG_DEVICE_SW_STATE_ON. When the usage of the device is complete and released, the same request with state set as MSG_DEVICE_SW_STATE_AUTO_OFF is invoked. Based on exclusive access request, multiple processing entities can share a specific hardware block, however, this must be carefully used keeping the full system view in mind.

```
n<b>Message</b>: #TISCI_MSG_SET_DEVICE n<b>Request</b>:
#tisci_msg_set_device_req n<b>Response</b>: #tisci_msg_set_device_resp
```

Syntax

```
int32_t Sciclient_pmSetModuleState(uint32_t moduleId,uint32_t state,uint32_t additionalFlag,uint32_t
timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

state : Module State requested. Refer ref Sciclient_PmSetDevice.

additionalFlag : Certain flags can also be set to alter the device state. Refer ref Sciclient_PmSetDeviceMsgFlags.

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.6 Sciclient_pmGetModuleState

Message to get the hardware block/Module state. This request does not require the processing entity to have control of the device via a set device state request.

```
n<b>Message</b>:                #TISCI_MSG_GET_DEVICE        n<b>Request</b>:
#tisci_msg_get_device_req n<b>Response</b>: #tisci_msg_get_device_resp
```

Syntax

```
int32_t Sciclient_pmGetModuleState(uint32_t moduleId,uint32_t * moduleState,uint32_t * reset-
State,uint32_t * contextLossState,uint32_t timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

moduleState : Module State returned. Refer ref Sciclient_PmGetDeviceMsgResp.

resetState : Programmed state of the reset lines.

contextLossState : Indicates how many times the device has lost context. A driver can use this monotonic counter to determine if the device has lost context since the last time this message was exchanged.

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.7 Sciclient_pmSetModuleRst

Set the device reset state. This is used to set or release various resets of the hardware block/module

```
n<b>Message</b>:                #TISCI_MSG_SET_DEVICE_RESETS
n<b>Request</b>:                #tisci_msg_set_device_resets_req  n<b>Response</b>:
#tisci_msg_set_device_resets_resp
```

Syntax

```
int32_t Sciclient_pmSetModuleRst(uint32_t moduleId,uint32_t resetBit,uint32_t timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

resetBit : Module Reset Bit to be set. TODO: Get reset IDs. Refer ref Sciclient_PmGetDeviceMsgResp. 1 - Assert the reset 0 - Deassert the reset Note this convention is opposite of PSC MDCTL

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.8 Sciclient_pmModuleClkRequest

Message to set the clock state: This requests for finer control of hardware device's clocks. This allows for configuration for hardware blocks that require customization of the specific input clocks. NOTE: each of the clock IDs are relative to the hardware block.

nMessage: #TISCI_MSG_SET_CLOCK nRequest: #tisci_msg_set_clock_req nResponse: #tisci_msg_set_clock_resp

Syntax

```
int32_t Sciclient_pmModuleClkRequest(uint32_t moduleId,uint32_t clockId,uint32_t state,uint32_t additionalFlag,uint32_t timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

clockId : Clock Id for the module. Refer ref Sciclient_PmModuleClockIds.

state : Clock State requested. Refer ref Sciclient_PmSetClockMsgState.

additionalFlag : Certain flags can also be set to alter the clock state. Refer ref Sciclient_PmSetClockMsgFlag.

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.9 Sciclient_pmModuleGetClkStatus

Message to get the clock state to or from a hardware block

nMessage: #TISCI_MSG_GET_CLOCK nRequest: #tisci_msg_get_clock_req nResponse: #tisci_msg_get_clock_resp

Syntax

```
int32_t Sciclient_pmModuleGetClkStatus(uint32_t moduleId,uint32_t clockId,uint32_t * state,uint32_t timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

clockId : Clock Id for the module. Refer ref Sciclient_PmModuleClockIds.

state : Clock State returned. Refer ref Sciclient_PmGetClockMsgState.

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.10 Sciclient_pmSetModuleClkParent

Message to Set Clock Parent: This message allows SoC specific customization for setting up a specific clock parent ID for the various clock input options for a hardware block's clock. This is rarely used customization that may be required based on the usecase of the system where the reset input clock option may not suffice for the usecase attempted.

```
n<b>Message</b>:                                #TISCI_MSG_SET_CLOCK_PARENT
n<b>Request</b>:                                #tisci_msg_set_clock_parent_req    n<b>Response</b>:
#tisci_msg_set_clock_parent_resp
```

Syntax

```
int32_t Sciclient_pmSetModuleClkParent(uint32_t moduleId,uint32_t clockId,uint32_t parent,uint32_t
timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

clockId : Clock Id for the module. Refer ref Sciclient_PmModuleClockIds.

parent : Parent Id for the clock. TODO: Find what this is.

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.11 Sciclient_pmGetModuleClkParent

Message to Get Clock Parent: Query the clock parent currently configured for a specific clock source of a hardware block This is typically used to confirm the current clock parent to ensure that the requisite usecase for the hardware block can be satisfied.

```
n<b>Message</b>:                                #TISCI_MSG_GET_CLOCK_PARENT
n<b>Request</b>:                                #tisci_msg_get_clock_parent_req    n<b>Response</b>:
#tisci_msg_get_clock_parent_resp
```

Syntax

```
int32_t Sciclient_pmGetModuleClkParent(uint32_t moduleId,uint32_t clockId,uint32_t * parent,uint32_t
timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

clockId : Clock Id for the module. Refer ref Sciclient_PmModuleClockIds.

parent : Returned Parent Id for the clock. TODO: Find what this is.

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.12 Sciclient_pmGetModuleClkNumParent

Message to get the number of clock parents for a given module. This is typically used to get the max number of clock parent options available for a specific hardware block's clock.

```
n<b>Message</b>:                #TISCI_MSG_GET_NUM_CLOCK_PARENTS
n<b>Request</b>:                #tisci_msg_get_num_clock_parents_req  n<b>Response</b>:
#tisci_msg_get_num_clock_parents_resp
```

Syntax

```
int32_t Sciclient_pmGetModuleClkNumParent(uint32_t moduleId,uint32_t clockId,uint32_t * numParent,uint32_t timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

clockId : Clock Id for the module. Refer ref Sciclient_PmModuleClockIds.

numParent : Returned number of parents.

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.13 Sciclient_pmSetModuleClkFreq

Message to set the clock frequency. This is typically desired when the default frequency of the hardware block's clock is not appropriate for the usecase desired. NOTE: Normally clock frequency management is automatically done by TISCI entity. In case of specific requests, TISCI evaluates capability to achieve requested range and responds with success/failure message. This sets the desired frequency for a clock within an allowable range. This message will fail on an enabled clock unless MSG_FLAG_CLOCK_ALLOW_FREQ_CHANGE is set for the clock. Additionally, if other clocks have their frequency modified due to this message, they also must have the MSG_FLAG_CLOCK_ALLOW_FREQ_CHANGE or be disabled.

```
n<b>Message</b>:                #TISCI_MSG_SET_FREQ                n<b>Request</b>:
#tisci_msg_set_freq_req n<b>Response</b>: #tisci_msg_set_freq_resp
```

Syntax

```
int32_t Sciclient_pmSetModuleClkFreq(uint32_t moduleId,uint32_t clockId,uint64_t freqHz,uint32_t additionalFlag,uint32_t timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

clockId : Clock Id for the module. Refer ref Sciclient_PmModuleClockIds.

freqHz : Frequency of the clock in Hertz.

additionalFlag : Additional flags for the request .Refer ref Tisci_PmSetClockMsgFlag .

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.14 Sciclient_pmQueryModuleClkFreq

Message to query the best clock frequency in the given range. This message does no real operation, instead, it requests the system control entity to respond with the best frequency that can match a frequency range provided. NOTE: This is a snapshot view. In a multi processing system, it is very well possible that another processing entity might change the configuration after one entity has queried for best match capability. Only a SET_CLOCK_FREQ will guarantee the frequency is configured.

```
n<b>Message</b>:          #TISCI_MSG_QUERY_FREQ      n<b>Request</b>:
#tisci_msg_query_freq_req n<b>Response</b>: #tisci_msg_query_freq_resp
```

Syntax

```
int32_t Sciclient_pmQueryModuleClkFreq(uint32_t moduleId,uint32_t clockId,uint64_t freqHz,uint32_t
timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.

clockId : Clock Id for the module. Refer ref Sciclient_PmModuleClockIds.

freqHz : Frequency of the clock in Hertz.

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.15 Sciclient_pmGetModuleClkFreq

Message to Get Clock Frequency This is most used functionality and is meant for usage when the driver controlling the hardware block requires to know the input clock frequency for configuring internal dividers / multipliers as required.

```
n<b>Message</b>:          #TISCI_MSG_GET_FREQ      n<b>Request</b>:
#tisci_msg_get_freq_req n<b>Response</b>: #tisci_msg_get_freq_resp
```

Syntax

```
int32_t Sciclient_pmGetModuleClkFreq(uint32_t moduleId,uint32_t clockId,uint64_t * freqHz,uint32_t
timeout);
```

Arguments

moduleId : Module for which the state should be set. Refer ref Sciclient_PmDeviceIds.
 clockId : Clock Id for the module. Refer ref Sciclient_PmModuleClockIds.
 freqHz : Frequency of the clock returned in Hertz.
 timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.16 Sciclient_pmEnableWdt

Enables the WDT controllers within the DMSC.

nMessage: #TISCI_MSG_ENABLE_WDT nRequest:
 #tisci_msg_enable_wdt_req nResponse: #tisci_msg_enable_wdt_resp

Syntax

```
int32_t Sciclient_pmEnableWdt(uint32_t timeout);
```

Arguments

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.17 Sciclient_pmDisableWakeup

This message is part of the CPU Off sequence. The sequence is: - Mask interrupts - Send wake reset message to PMMC - Wait for wake reset ACK - Abort if any interrupts are pending - Disable all interrupts - Send goodbye to PMMC - Wait for goodbye ACK - Execute WFI

nMessage: #TISCI_MSG_WAKE_RESET nRequest:
 #tisci_msg_wake_reset_req nResponse: #tisci_msg_wake_reset_resp

Syntax

```
int32_t Sciclient_pmDisableWakeup(uint32_t timeout);
```

Arguments

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.18 Sciclient_pmGetWakeupReason

Request wakeup reason After a wakeup, the host can request the deepest sleep/idle mode reached and the reason for the wakeup. The API also returns the time spent in idle state.

nMessage: #TISCI_MSG_WAKE_REASON nRequest:
#tisci_msg_wake_reason_req nResponse: #tisci_msg_wake_reason_resp

Syntax

```
int32_t Sciclient_pmGetWakeupReason(uint8_t mode[32],uint8_t reason[32],uint32_t * time_ms,uint32_t timeout);
```

Arguments

mode[32] : Deepest sleep/idle mode 0x000C reached (ASCII)

reason[32] : Wakeup reason (ASCII)

time_ms : Time spent in idle state (ms)

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.19 Sciclient_pmDevicePowerOff

Some processors have a special sequence for powering off the core that provides notification to the PMMC when that sequence has completed. For processors without such a sequence, the goodbye message exists. The exact sequence involved in the goodbye message depends on the SoC.

nMessage: #TISCI_MSG_GOODBYE nRequest:
#tisci_msg_goodbye_req nResponse: #tisci_msg_goodbye_resp

Syntax

```
int32_t Sciclient_pmDevicePowerOff(uint32_t timeout);
```

Arguments

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.20 Sciclient_pmDeviceReset

Objective: Trigger a SoC level reset Usage: Used to trigger a system level reset. NOTE: Depending on permissions configured for the SoC, not all processing entities may be permitted to request a SoC reset. When permitted, the request once processed will not return back to caller.

nMessage: #TISCI_MSG_SYS_RESET nRequest:
#tisci_msg_sys_reset_req nResponse: #tisci_msg_sys_reset_resp

Syntax

```
int32_t Sciclient_pmDeviceReset(uint32_t timeout);
```

Arguments

timeout : Gives a sense of how long to wait for the operation. Refer ref Sciclient_ServiceOperationTimeout.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

4.3.21 Sciclient_pmIsModuleValid

This API would check if the given module Id is valid for the device. The module Id that is referred to is ref Sciclient_PmDeviceIds.

Syntax

```
int32_t Sciclient_pmIsModuleValid(uint32_t modId);
```

Arguments

modId : Module Index to be checked.

Return Value CSL_PASS on success, else failure

Comments None

Constraints None

See Also None

DESIGN ANALYSIS AND RESOLUTION(DAR)

5.1 DAR Criteria 1

SCIClient should support OS and non OS applications. However, SCIClient in an OS context should be able to prevent multiple threads from writing to the secure proxy.

5.1.1 Available Alternatives

5.1.1.1 Alternative 1

Built the library separately for OS and non OS. Each API will have its own OS and Non-OS implementation.

5.1.1.2 Alternative 2

Use PDK OSAL and have the OSAL support for non-OS and OS implementation. The SCIClient APIs will have one implementation. The application should link OSAL as well.

5.1.2 Decision

Use Alternative 2 as the OSAL already has OS and non-OS implementation. The SCIClient need not duplicate code. Consistent with other libraries as well.

5.2 DAR Criteria 2

SCIClient constructing the SCI core message based on fields given as input by the higher level software.

5.2.1 Available Alternatives

5.2.1.1 Alternative 1

SCIClient maintains separate APIs for all the message types possible and the PM/RM/Security Libs pass parameters to this. Eg. So if a SCI message looks like

```
struct msg_rm_alloc_foo {
    struct message_hdr hdr;
    s32 param_a;
    u16 param_b;
```

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```
    u16 param_c;  
} __attribute__((__packed__));
```

The SCILIB API looks something like

```
int32_t sci_client_rm_alloc_foo(int32_t param_a, uint16_t param_b, uint16_t param_c);
```

SCILIB abstracts the packed message format and the header details.

5.2.1.2 Alternative 2

SCI message structure is instead of

```
struct msg_rm_alloc_foo {  
    struct message_hdr hdr;  
    s32 param_a;  
    u16 param_b;  
    u16 param_c;  
} __attribute__((__packed__));  
  
int32_t sci_client_rm_alloc_foo(int32_t param_a, uint16_t param_b, uint16_t param_c);
```

Do the following

```
struct msg_rm_alloc_foo_body {  
    s32 param_a;  
    u16 param_b;  
    u16 param_c;  
} __attribute__((__packed__));  
  
int32_t sci_client_rm_alloc_foo(const struct msg_rm_alloc_foo_body * body);
```

Just to extend that a bit further:

```
int32_t sci_client_rm_alloc_foo(const struct msg_rm_alloc_foo_body * body);
```

becomes a common API

```
int32_t sci_client_send_message(uint32_t message_type, const struct void * body);
```

Apart from message_type we have some more inputs which we finally capture in an inPrm structure.

5.2.2 Decision

Use alternate 2 to not have multiple APIs in the SCIClient HAL and the SCIClient HAL will expose the core message structure for the higher level software to work on . Above this, SCIClient FL will have separate API definitions for each type of supported message separately for PM, RM and Security .

DOCUMENT REVISION HISTORY

Version #	Date	Author Name	Revision History	Status
01.00	2-Jan-2018	SACHIN PURO- HIT	Added design info for sciclient.h	Draft